



RF/mm and Programmable Photonics

José Capmany

Cadence Photonics Summit and Workshop
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Agenda

01 Introduction

02 RF/mm Photonics

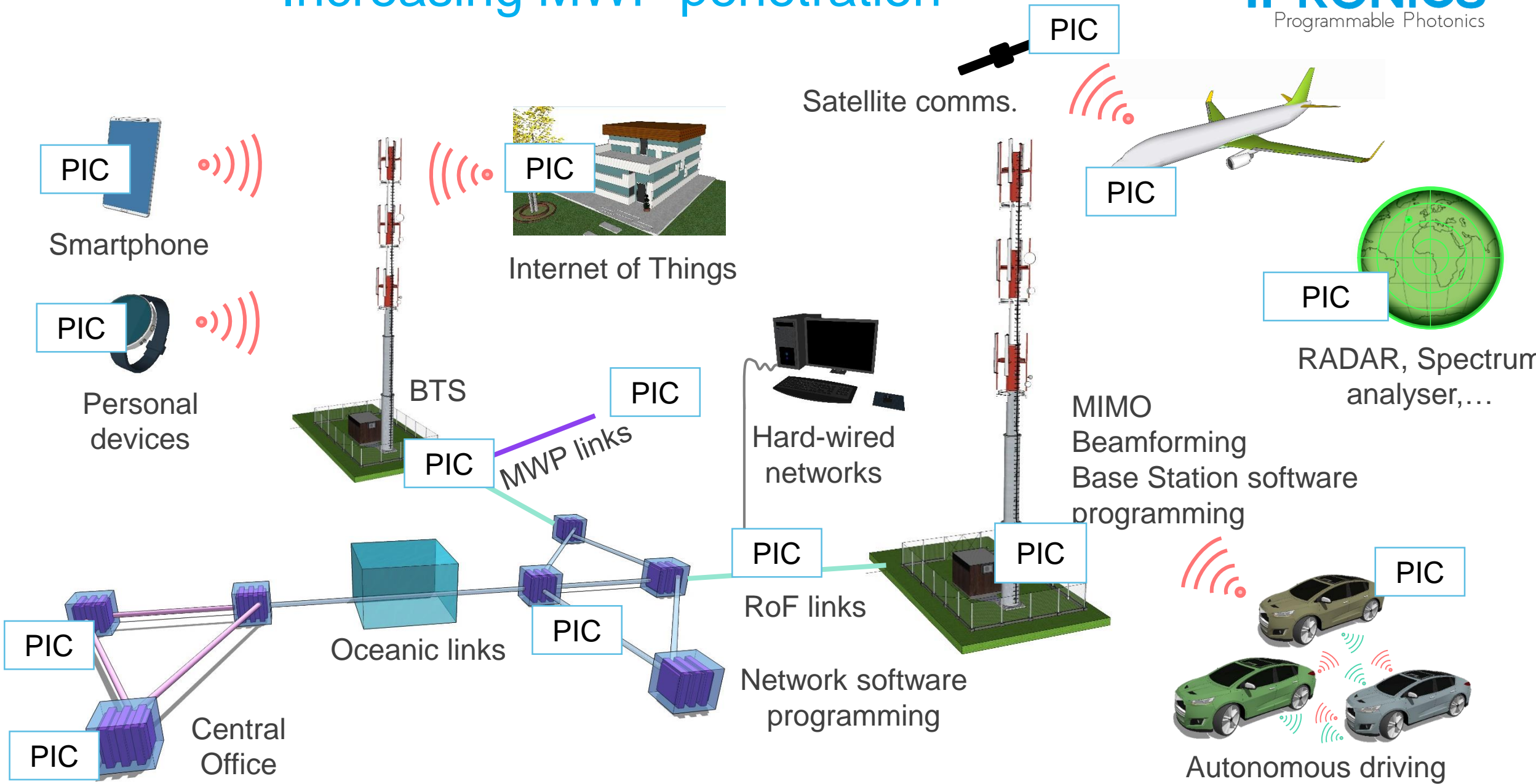
03 Programmable
Integrated Photonics

04 Summary &
Conclusions

Introduction



Increasing MWP penetration



RF/mm Photonics

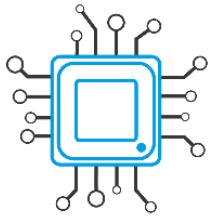
Integrated MWP





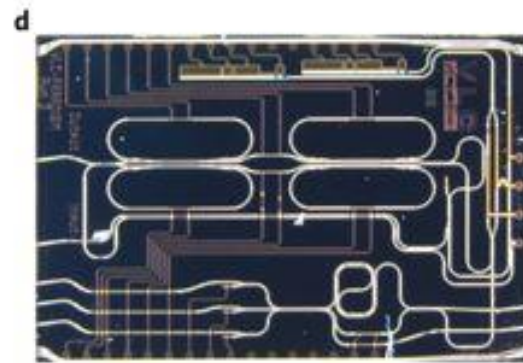
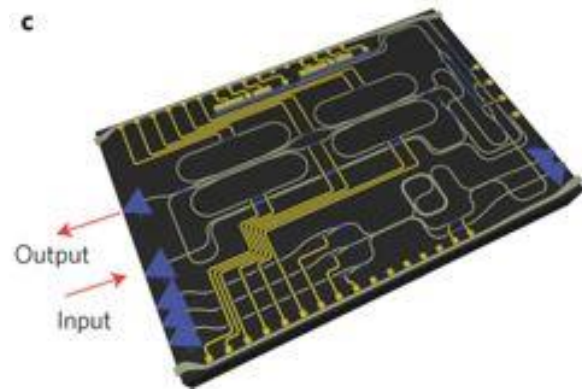
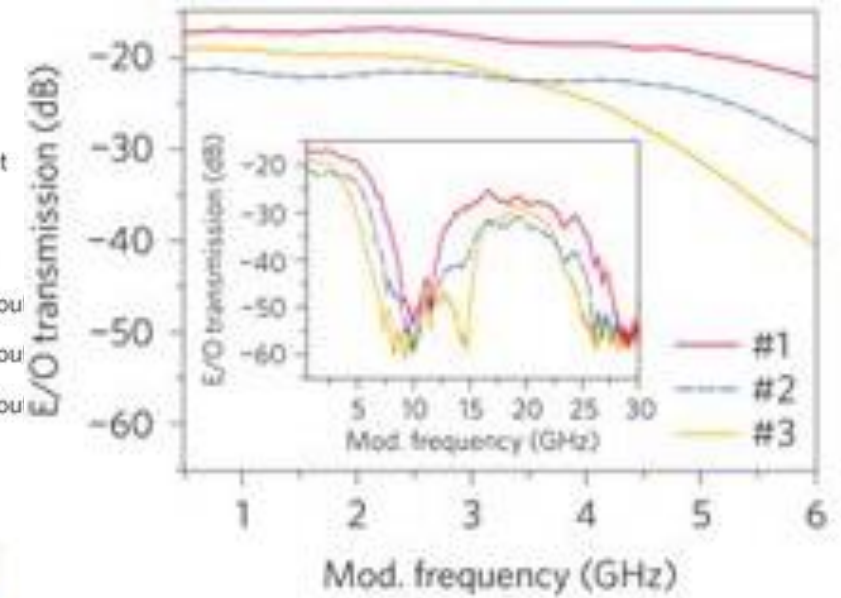
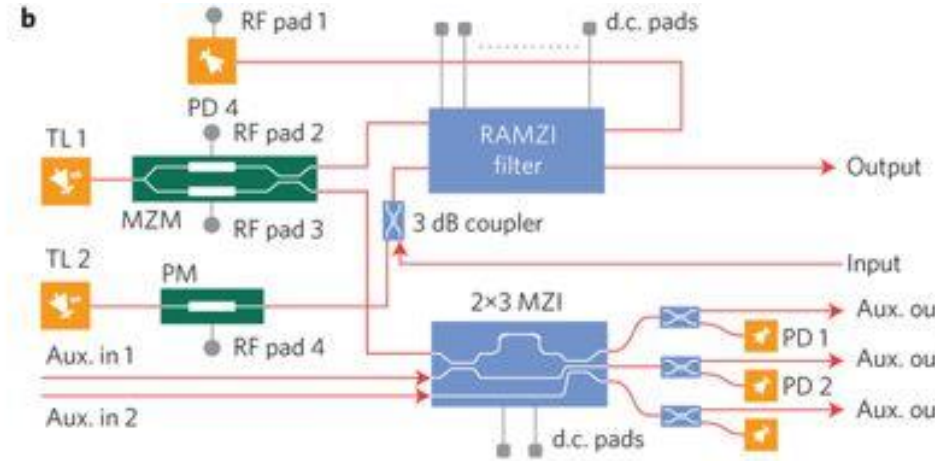
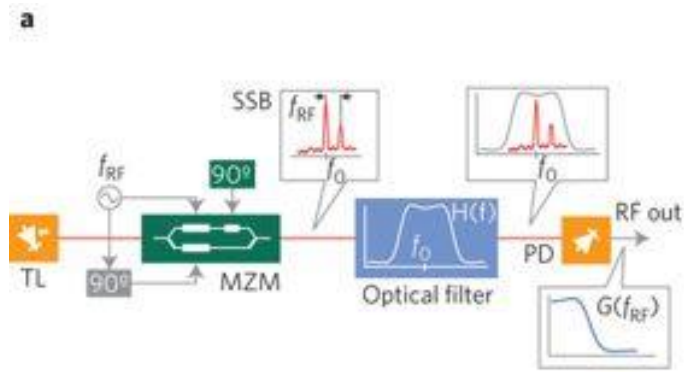
IMWP ASPICS

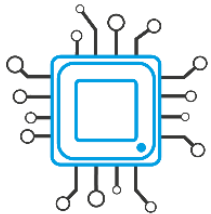
- Designed to carry only a given functionality
- Feature some degree of flexibility enabled tuning some of its internal parameters by means of appropriate control signals.
- Fixed physical topology.
- A considerable amount of circuits reported in the literature (SOI, InP, SiN)
 - Filters
 - Delay lines
 - RF phase shifters
 - Switches, Add/Drop MuXes
 - Beamformers
 - Arbitrary waveform generators
 - Optoelectronic oscillators



IMWP ASPICS

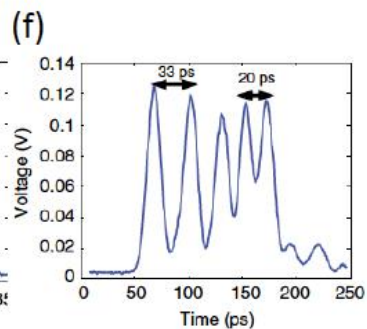
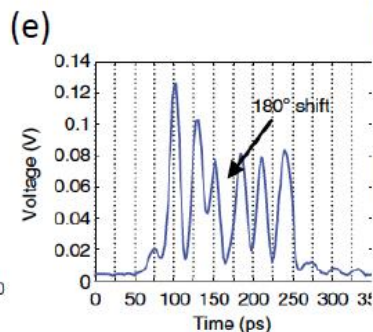
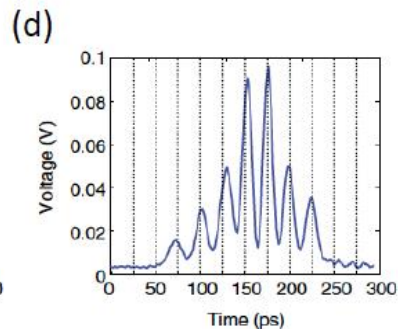
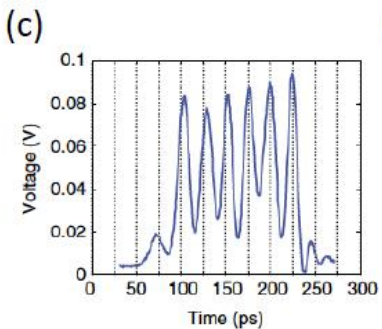
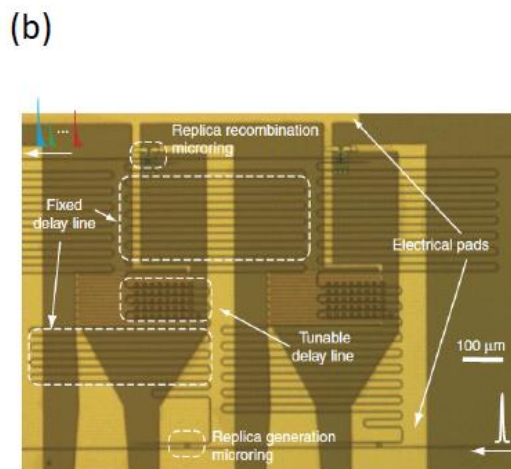
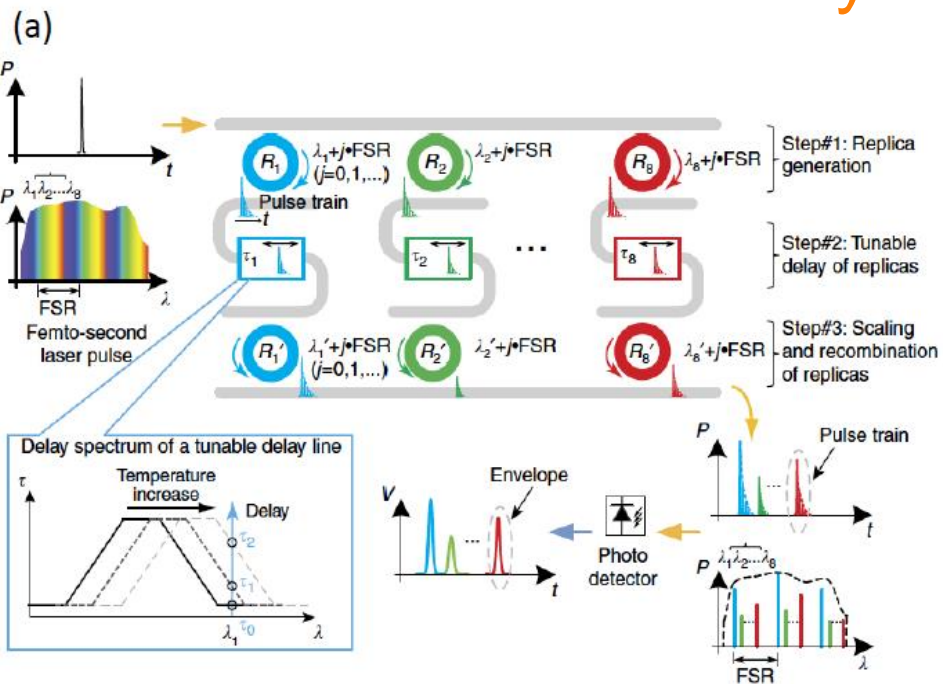
Reconfigurable Filters



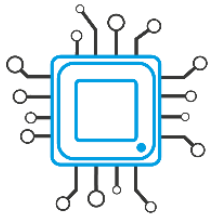


IMWP ASPICS

Tunable Arbitrary waveform generator

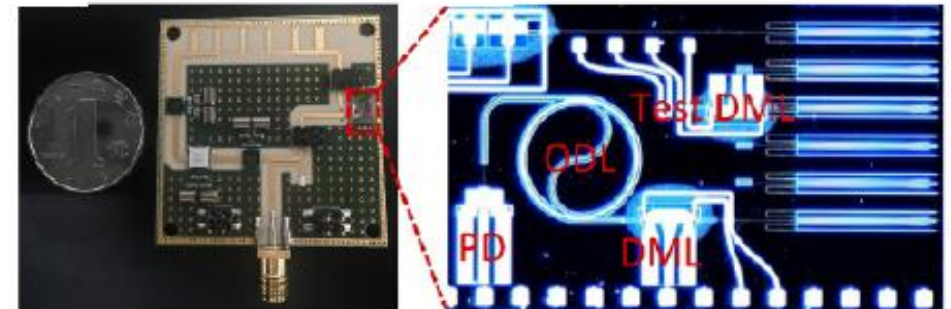
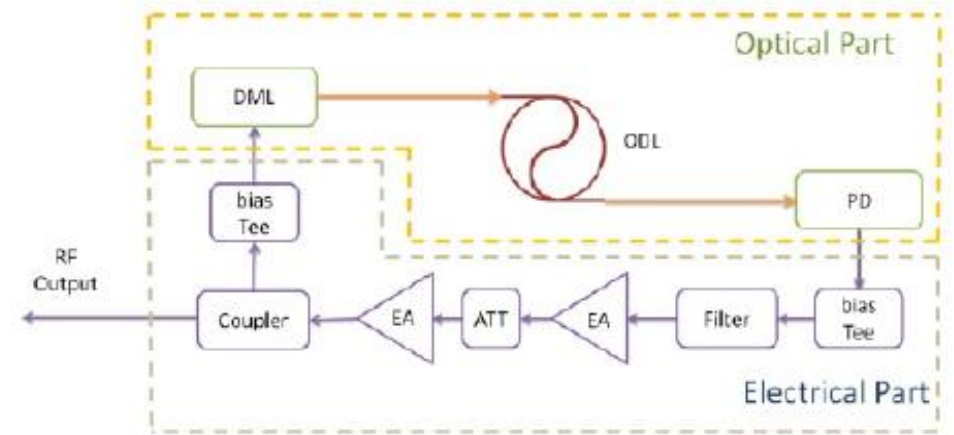
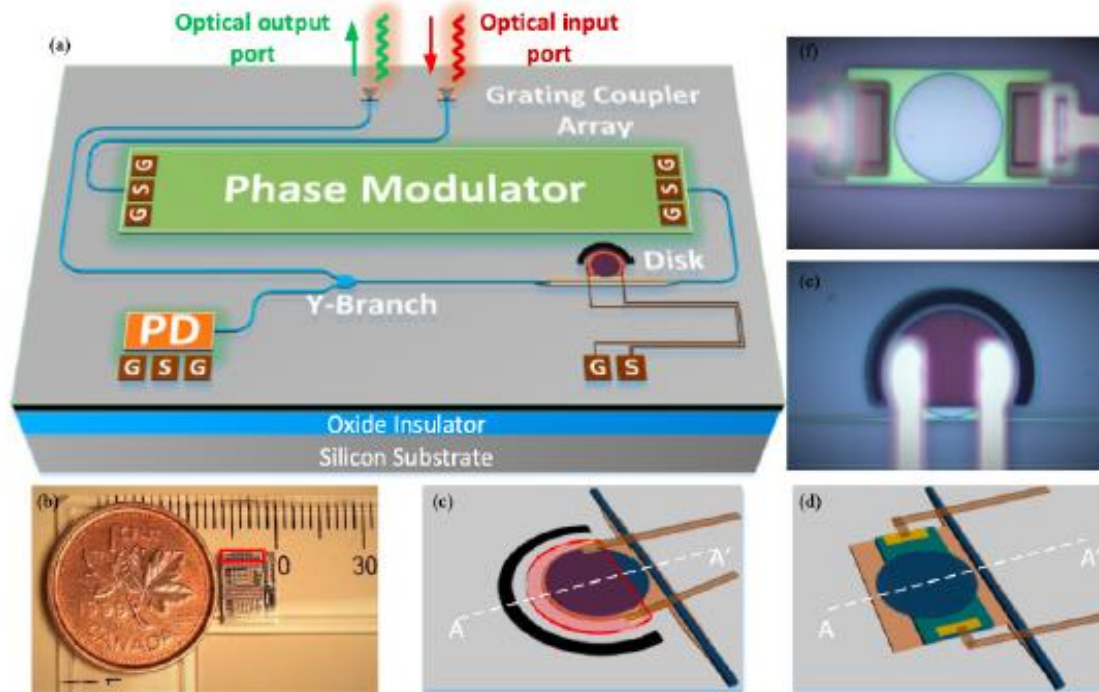


J. Wang et al., "Reconfigurable radio-frequency arbitrary waveforms synthesized in a silicon photonic chip," *Nature Comms.* 6, 5957 (2015).



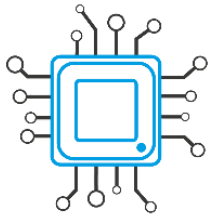
IMWP ASPICS

Optoelectronic Oscillators



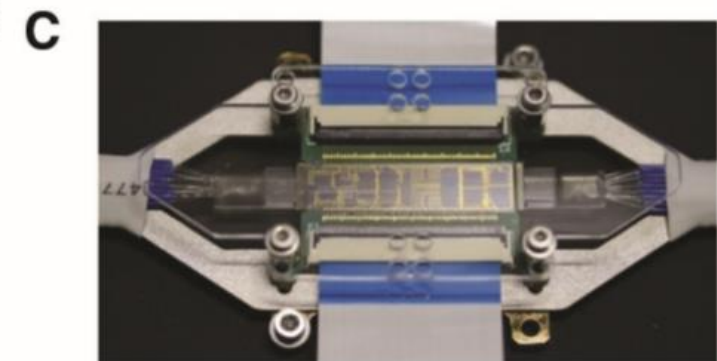
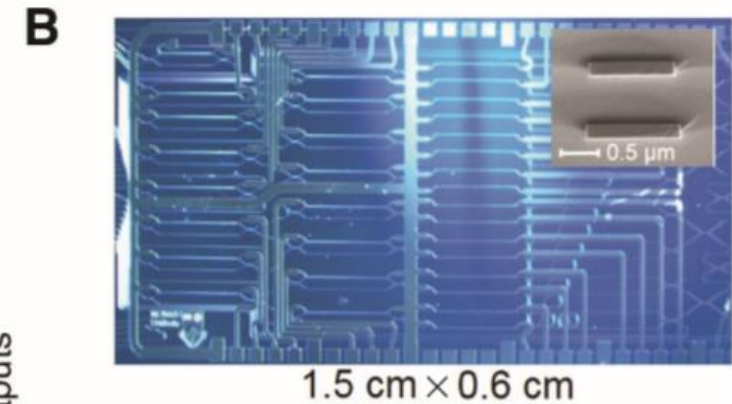
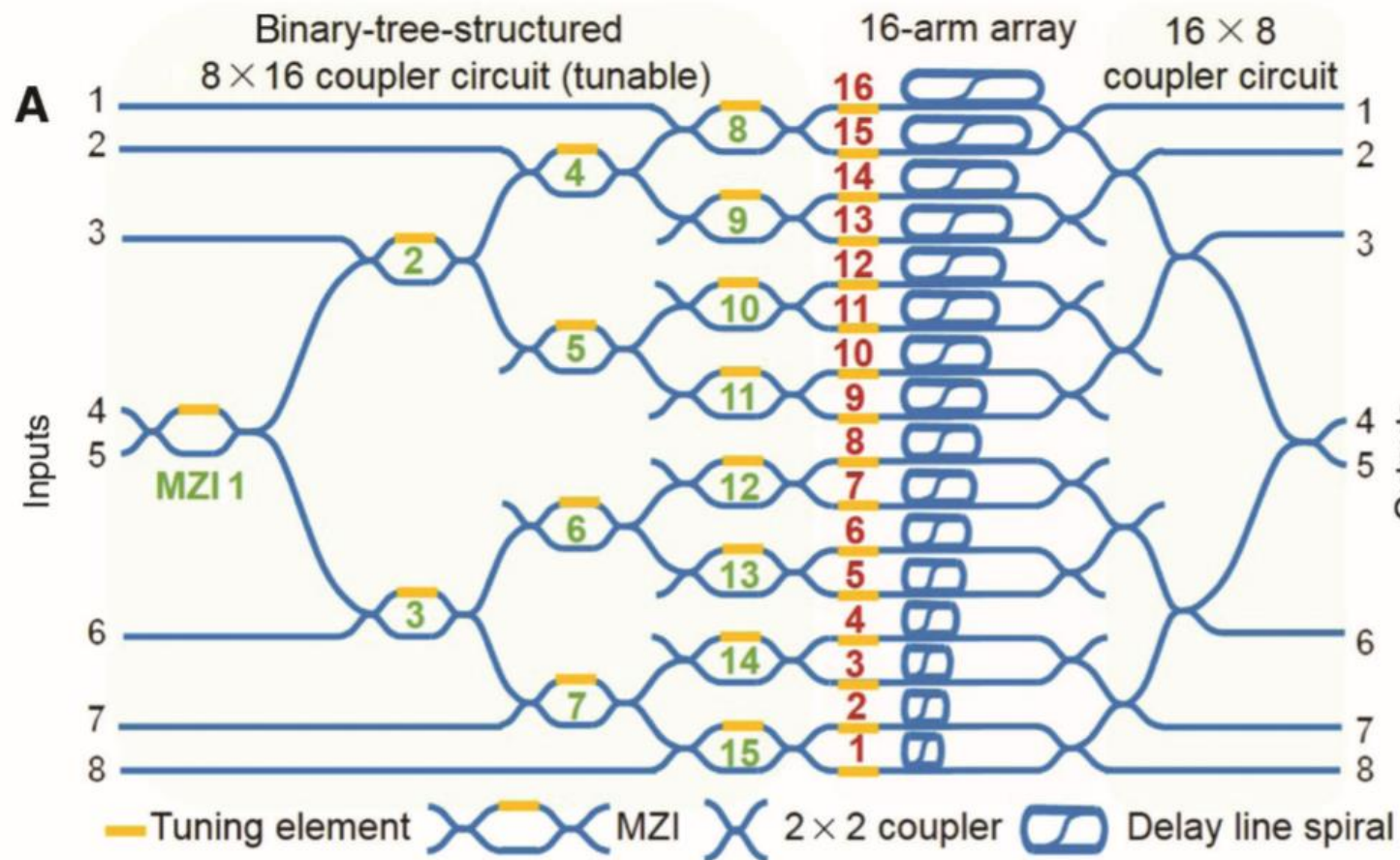
J. Tang, et al., Opt. Express 26, 12257-12265 (2018).

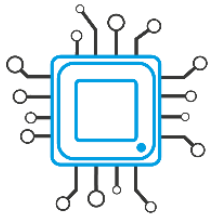
W. Zhang, J. Yao, IEEE J. Lightwave Tech. 36, 4655-4663, (2018).



IMWP Multiport circuits

Signal Processors & Beamformers





IMWP ASICS

Comprehensive Reviews



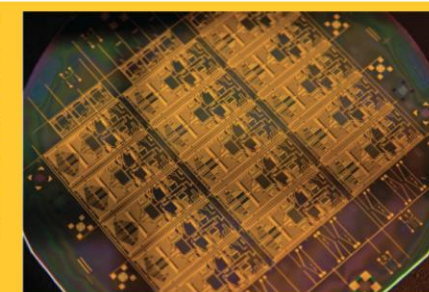
2013

LASER & PHOTONICS REVIEWS

Laser Photonics Rev. 7, No. 4, 506–538 (2013) / DOI 10.1002/lpor.201200032

REVIEW
ARTICLE

Abstract Microwave photonics (MWP) is an emerging field in which radio frequency (RF) signals are generated, distributed, processed and analyzed using the strength of photonic techniques. It is a technology that enables various functionalities which are not feasible to achieve only in the microwave domain. A particular aspect that recently gains significant interests is the use of photonic integrated circuit (PIC) technology in the MWP field for enhanced functionalities and robustness as well as the reduction of size, weight, cost and power consumption. This article reviews the recent advances in this emerging field which is dubbed as integrated microwave photonics. Key integrated MWP technologies are reviewed and the prospective of the field is discussed.



Integrated microwave photonics

David Marpaung^{1,4,*}, Chris Roeloffzen¹, René Heideman², Arne Leinse², Salvador Sales³, and José Capmany^{3,5}

REVIEW ARTICLE

<https://doi.org/10.1038/s41566-018-0310-5>

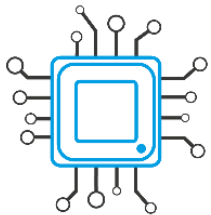
nature
photonics

2019

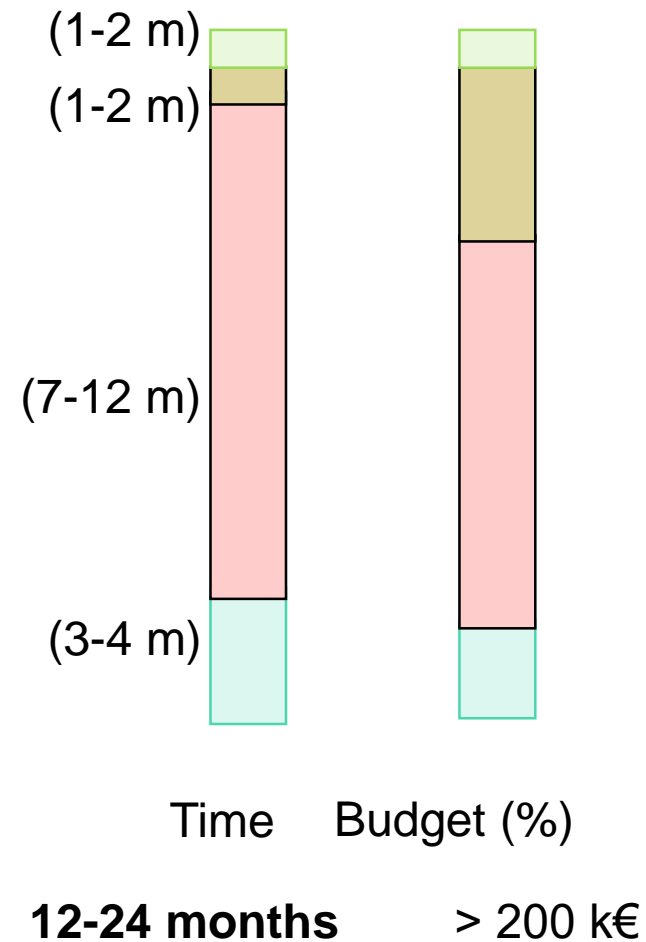
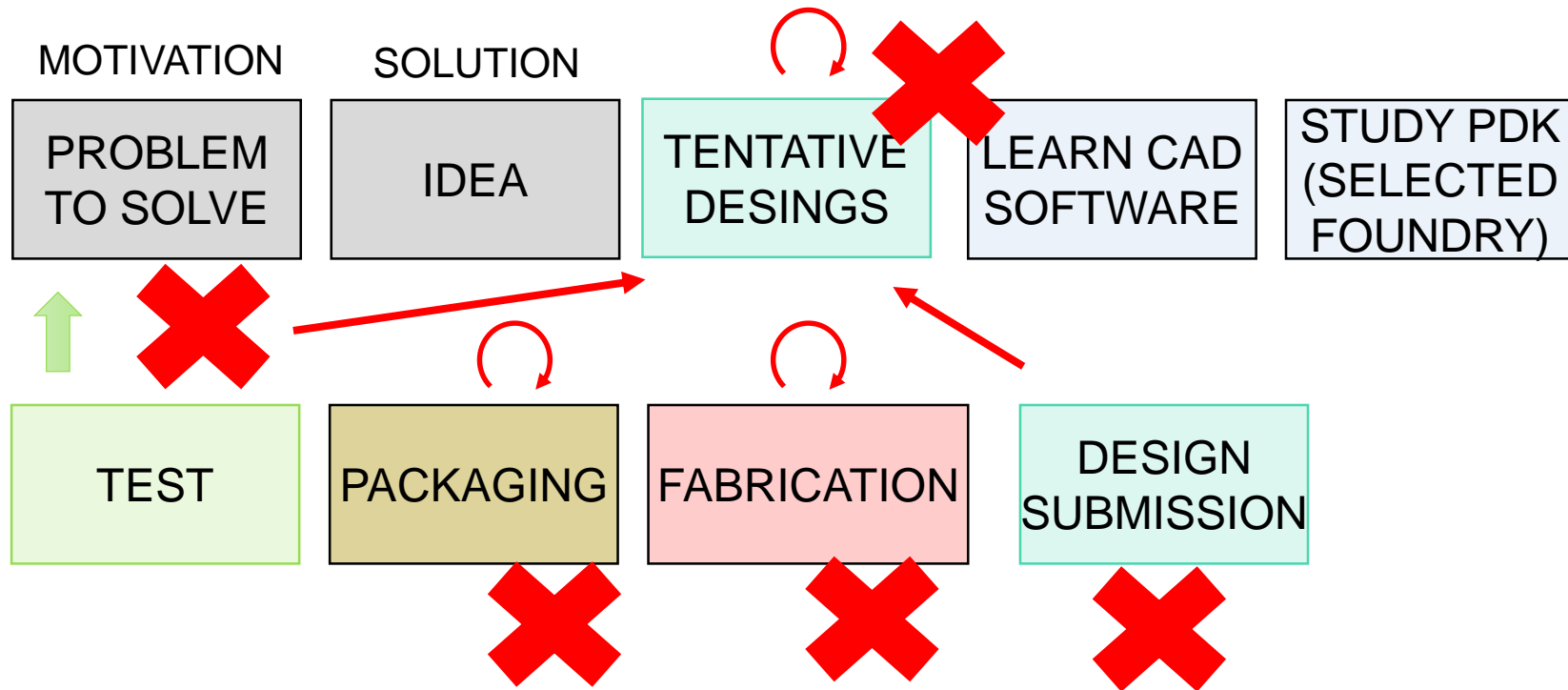
Integrated microwave photonics

David Marpaung ^{1*}, Jianping Yao ² and José Capmany³

NATURE PHOTONICS | VOL 13 | FEBRUARY 2019 | 80–90 | www.nature.com/naturephotonics



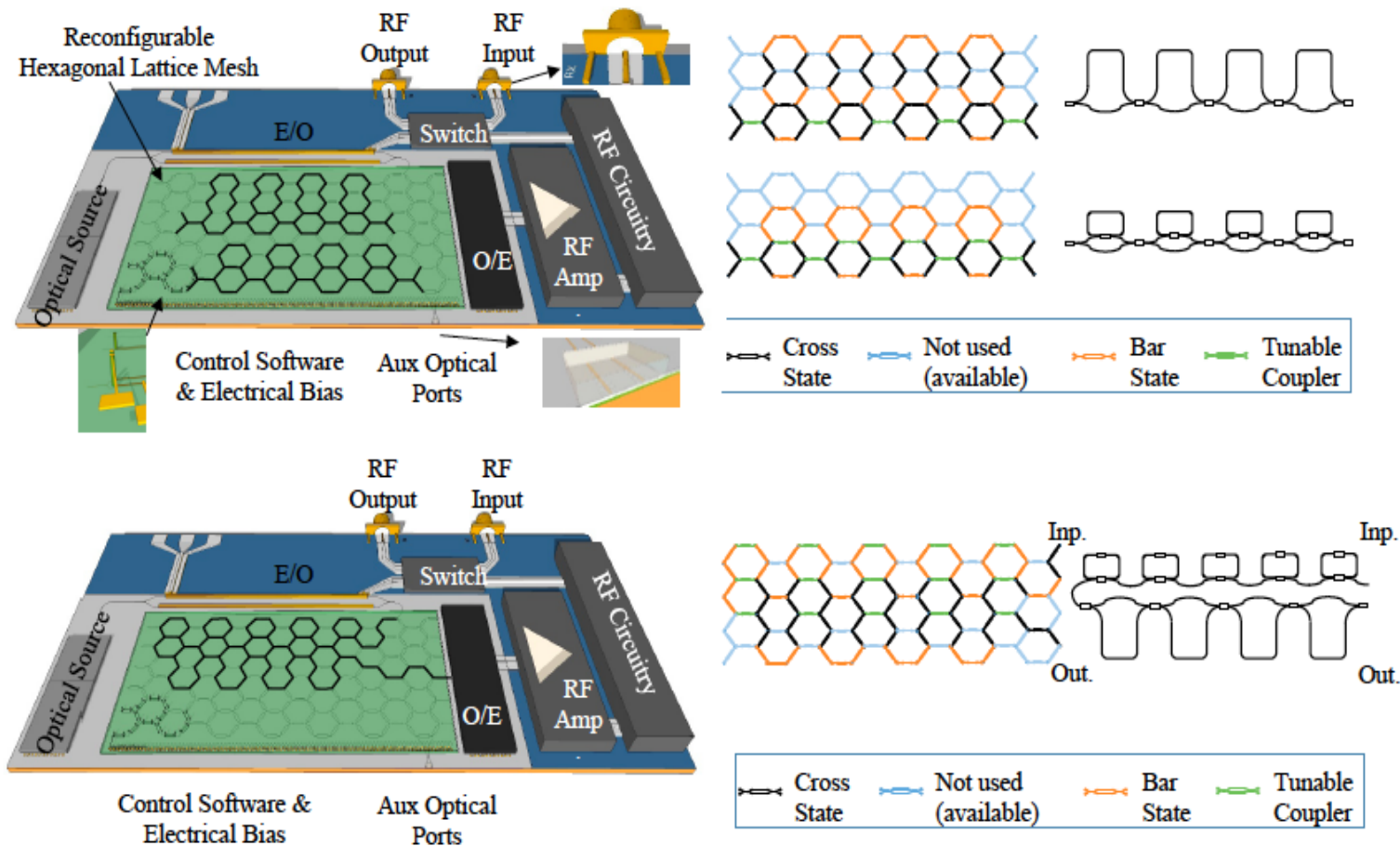
ASPIC Limitations



A failure at any stage origins iteration loops in the design procedure

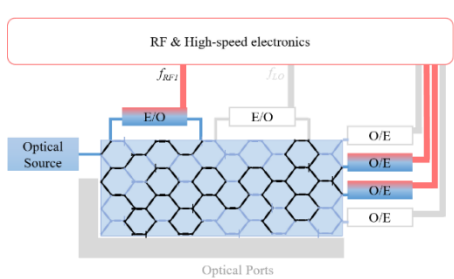
Iteration runs no included

The main objective of UMWP-CHIP is the design, implementation and validation of a universal integrated microwave photonics programmable signal processor, capable of performing the most important MWP functionalities featuring unique broadband and performance metrics,

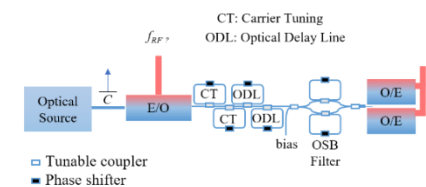


Target functionalities

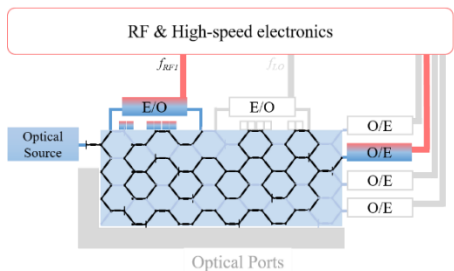
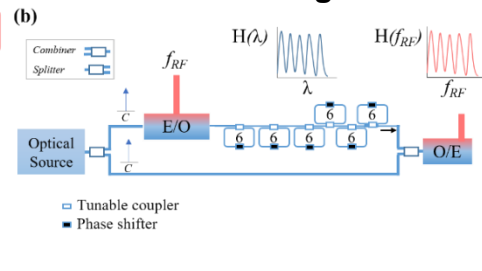
Wavelength to time mapping AWG



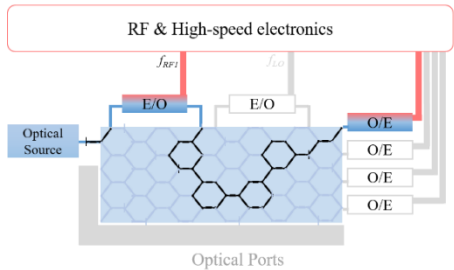
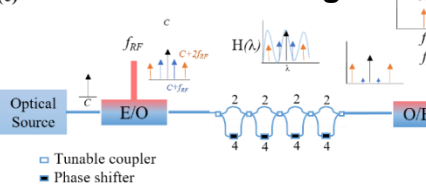
(a) **SCT True Time Delay Line**



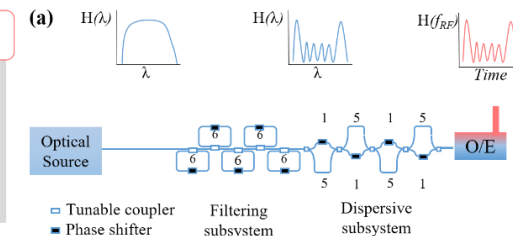
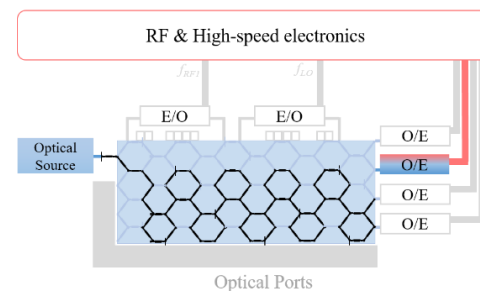
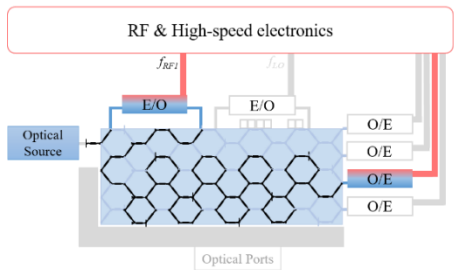
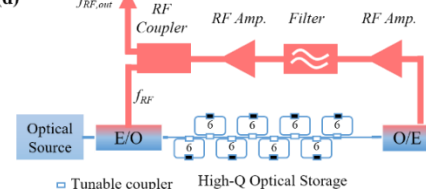
Self beating Rf Filter



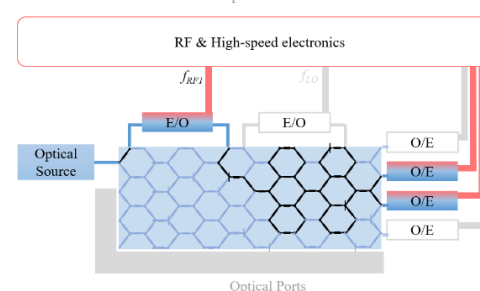
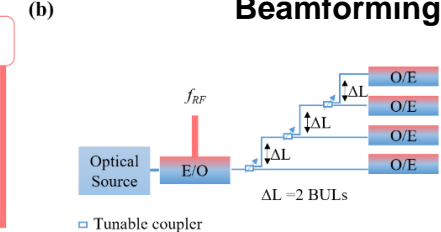
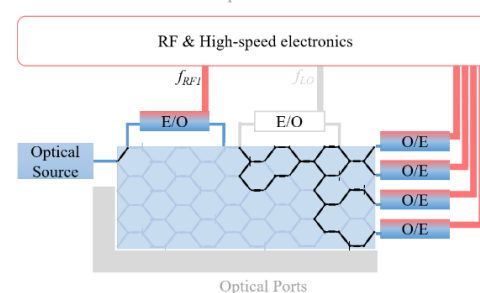
(c) **mm-wave tone generator**



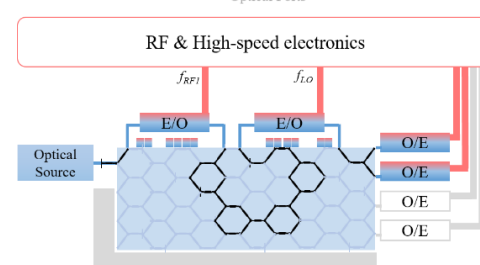
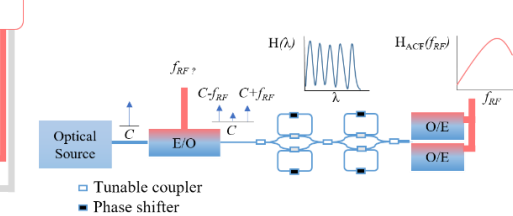
(d) **OEO**



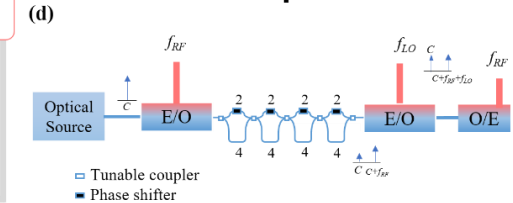
(b) **Beamforming network**



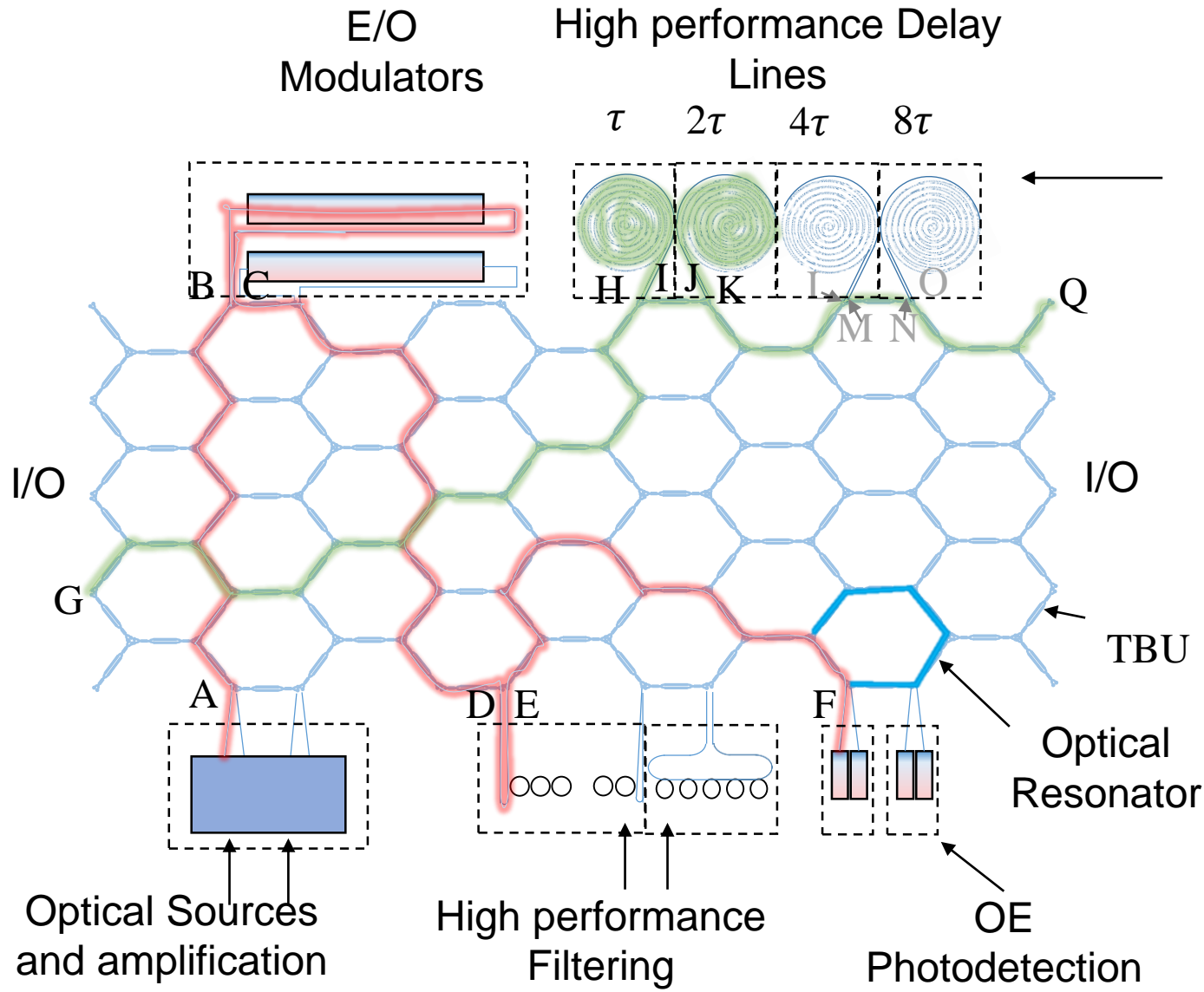
(c) **Instantaneous freq measurement**



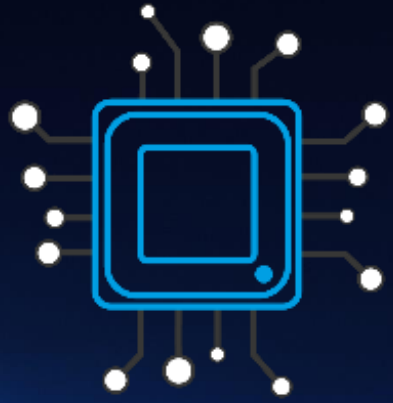
(d) **Up/down converter**



Outsourcing special blocks outside the core

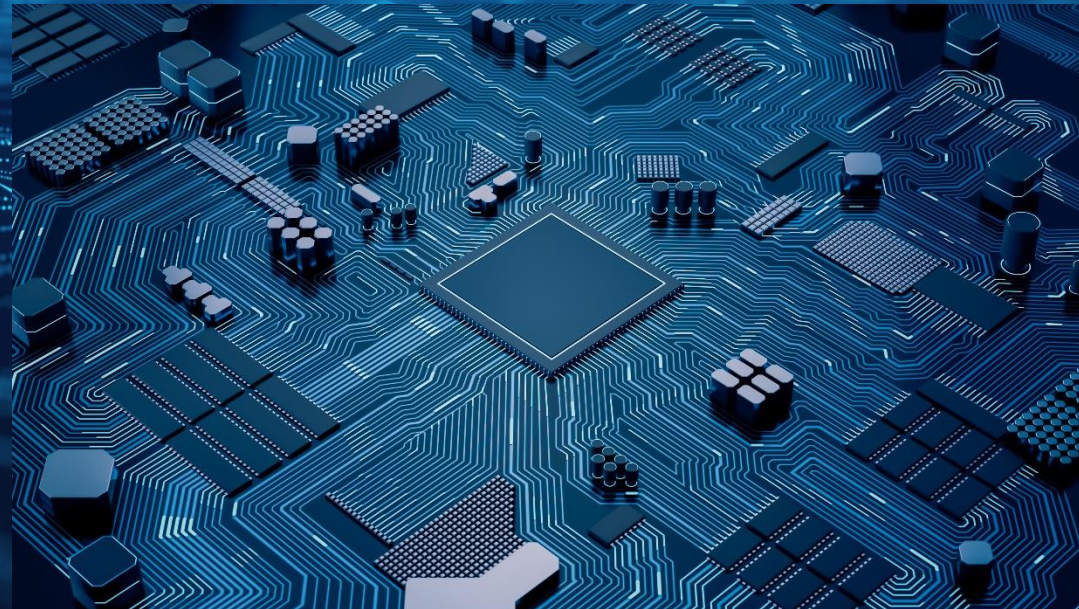


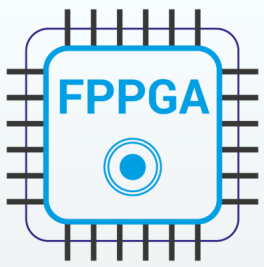
This configuration is novel in photonics, but certainly not (with some important differences) in electronics



Programmable Electronics vs Photonics

Some comparisons and lessons





Reusability in ITC systems

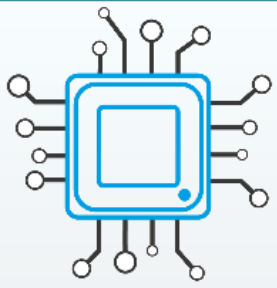
Re-usability / versatility / flexibility / Programmability are key features in past and future revolutions

SpaceX believes a fully and rapidly **reusable** rocket is the pivotal breakthrough needed to substantially reduce the cost and reduced development times of space access:

*“60 000 000 \$ total project cost, used 1000 times, becomes **three-order magnitude reduction** in space missions' costs.”*

- In **Electronics**: FPGAs instead of ASICs
- In **networks**: SDN instead of ad-hoc topologies and configurations
- In **radio**: Software radio instead of specific RF receivers



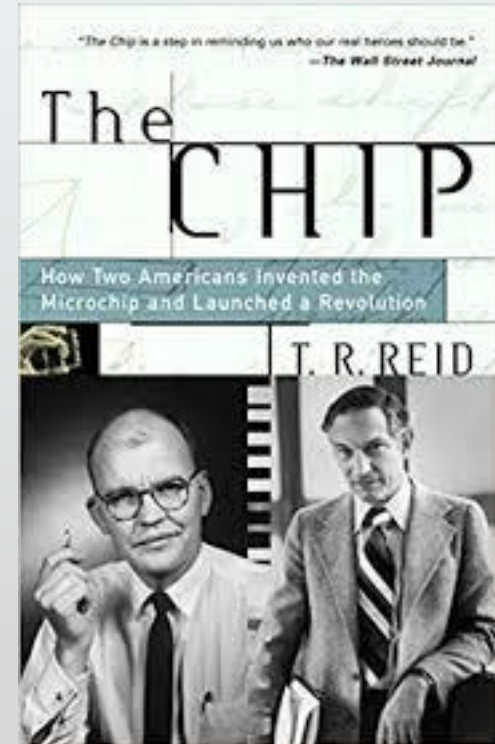


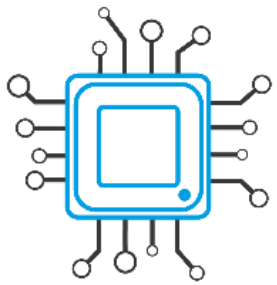
Birth of Programmable Electronics

....By the end of the sixties, Noyce was worried about the rapid proliferation of different integrated circuits, each designed for its own special purpose.....

...Looking ahead, Noyce saw that the solution to proliferation of special-purpose integrated circuits would be the development of general-purpose chips that could be manufactured in huge quantities and adapted (“programmed”) for specific applications.

T.R. Reid “The Chip: How Two Americans Invented the Microchip and Launched a Revolution”





FPGA Fast Refresher

FPGAs are mainly built using **irreversible 2x1 gates** defined by truth tables
 FPGAs work with **digital signals** and **Boolean Algebra**

Example of a 3x3 Logic Element CLA with 12 I/O pads & 3 types of L. E.'s

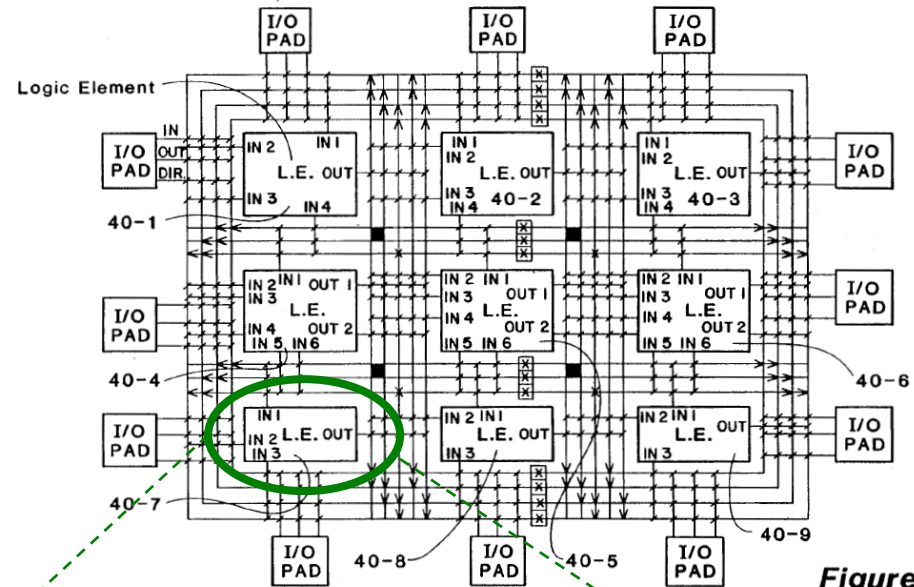


Figure 4A

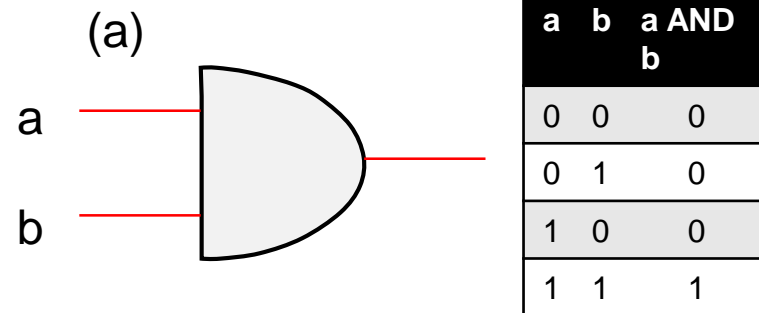


James Barnett

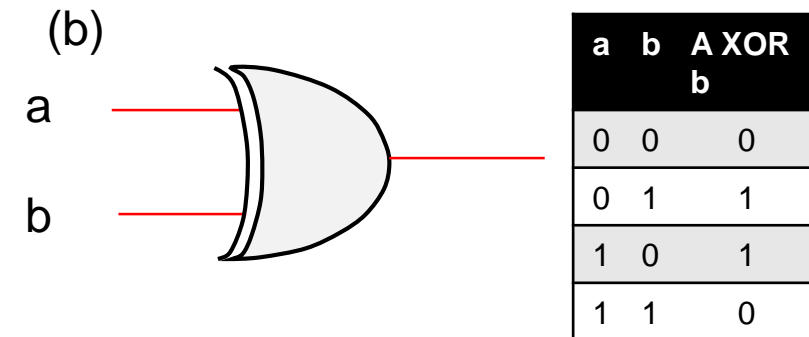
Ross Freeman

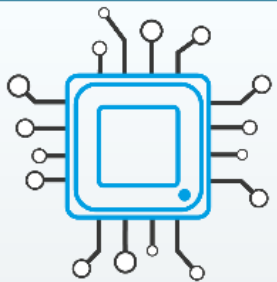
Bernie Voderschmitt

a AND b



a XOR b

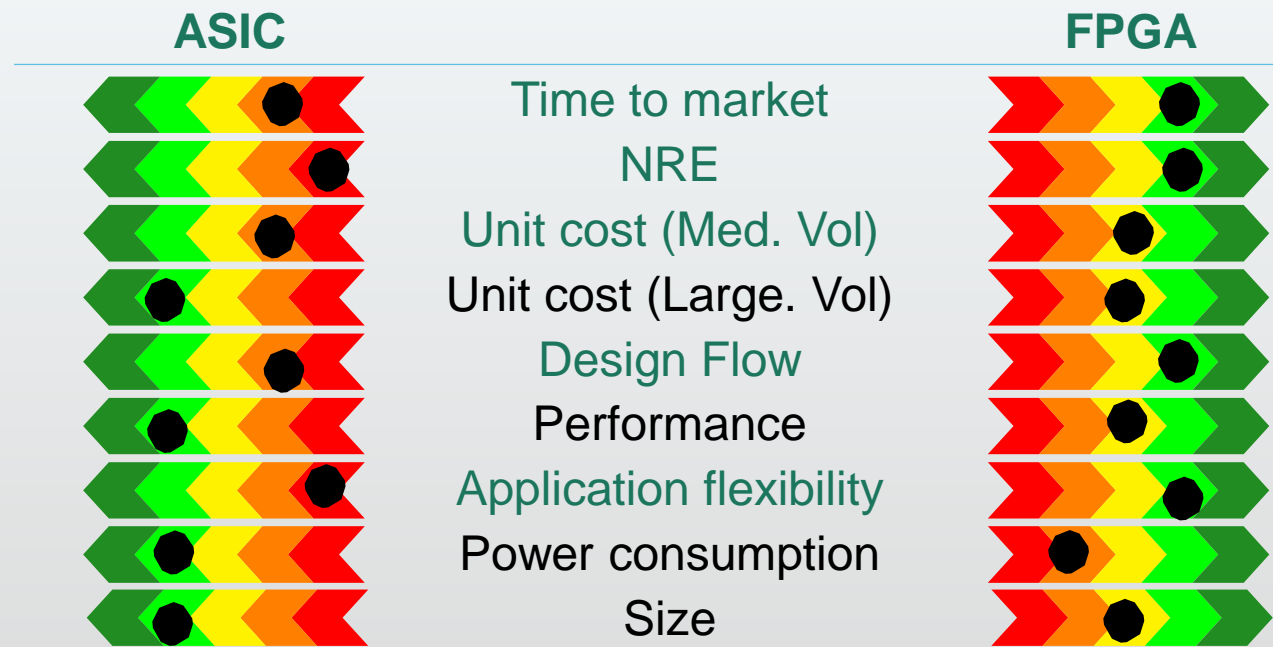




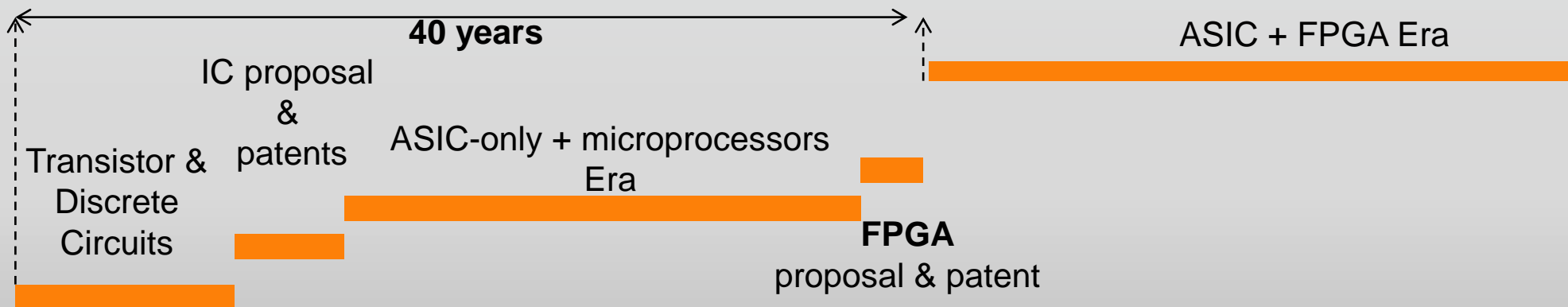
Why FPGAS in Electronics?

Electronic Integrated Circuit second revolution: reconfigurable ICs.

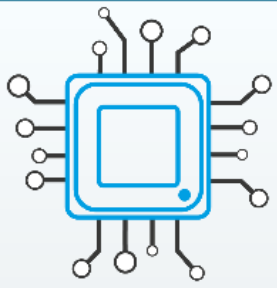
Currently, programmable and multipurpose EICs represent more than 50% of the market.



Electronics



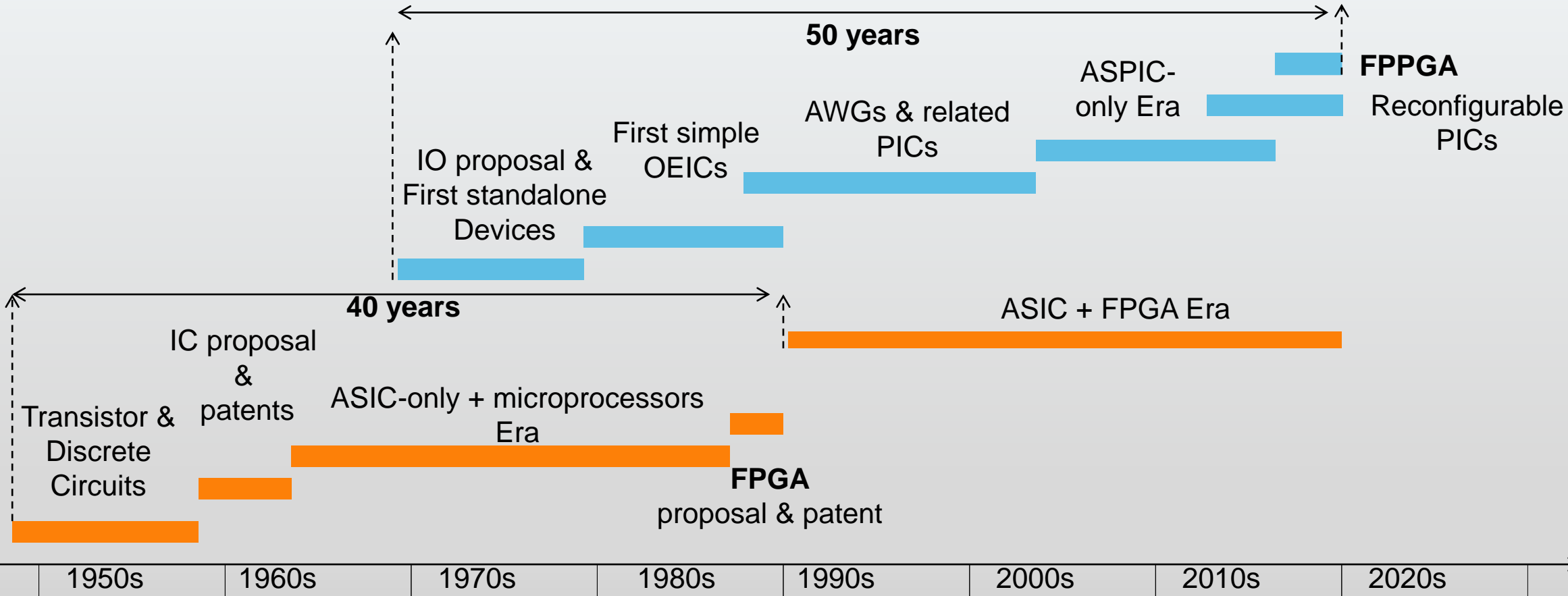
1940s	1950s	1960s	1970s	1980s	1990s	2000s	2010s	2020s
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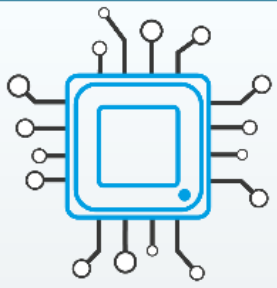


Electronics/Photonics: a parallel evolution?

Photonics

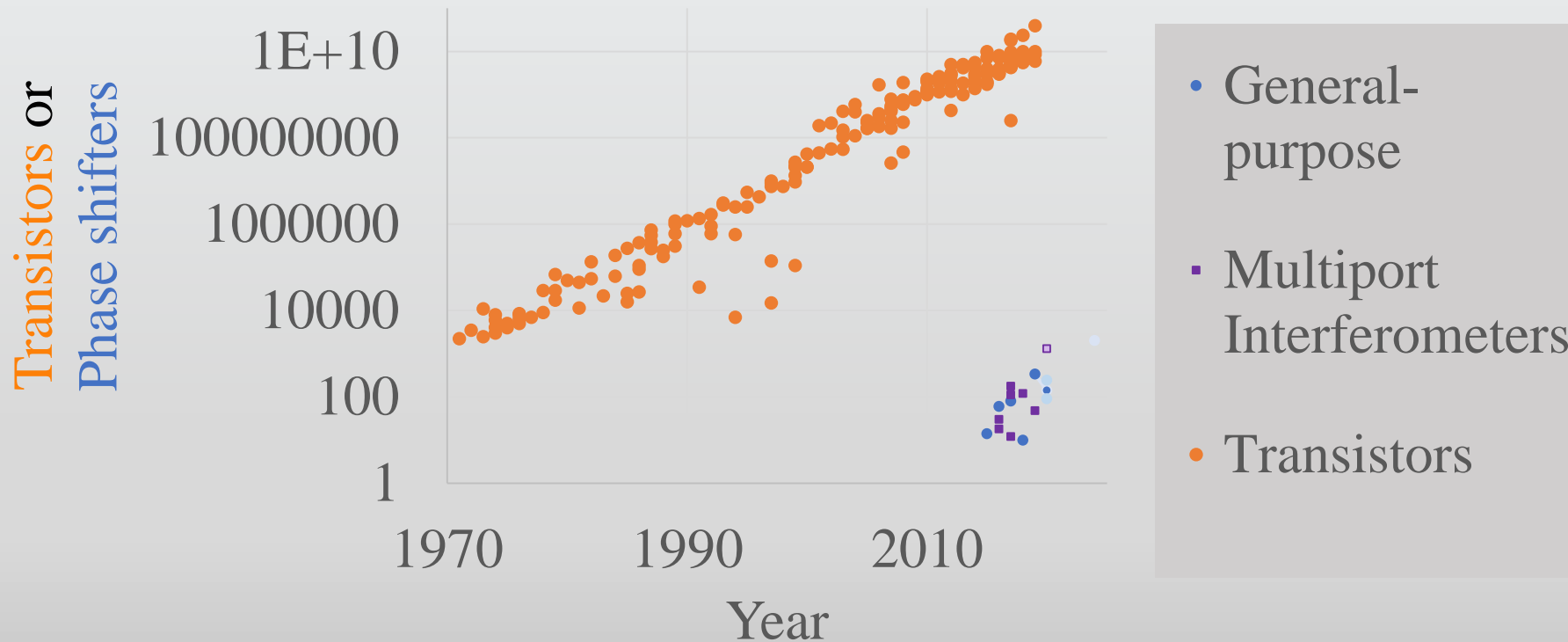
Electronics

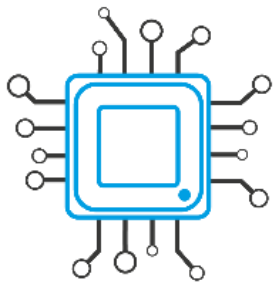




Electronics/Photonics: a parallel evolution?

Are we in front of another observational law in semiconductor technologies?





Evolution steps in Programmable Photonics

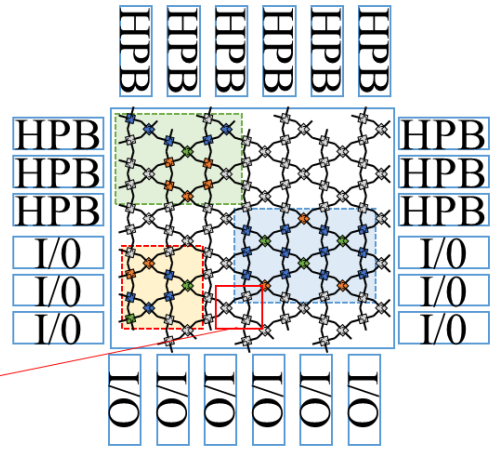
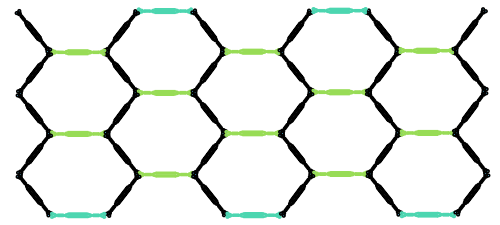
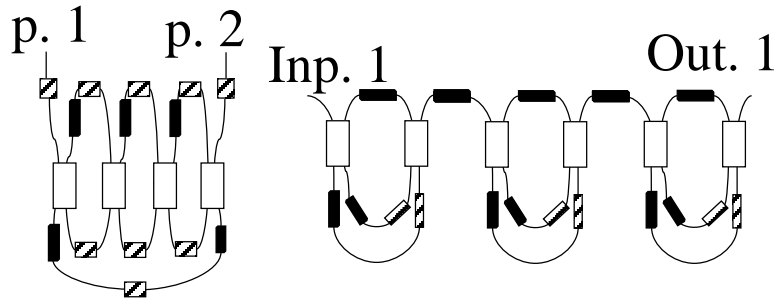
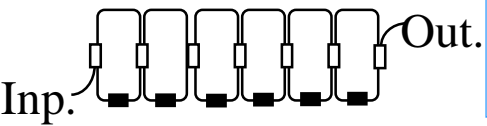
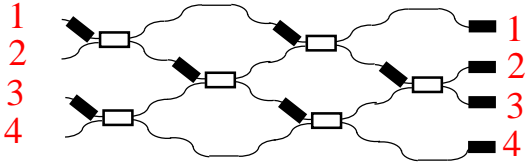
FPPGA

Programmable Multifunctional PICs

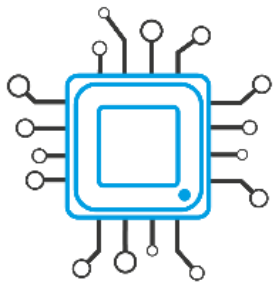
Multiport Interferometers

FEW-FUNCTIONAL ASPICS

Reconfigurable ASPICS



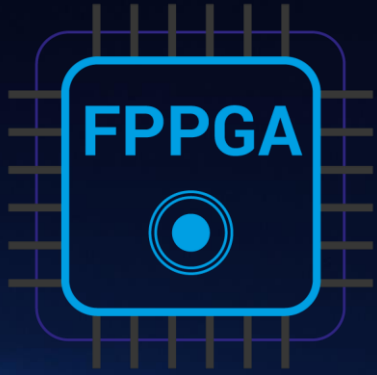
Semiconductor Optical Amplifier (SOA) Phase shifter Tunable Coupler



Some Relevant Literature in Programmable Photonics

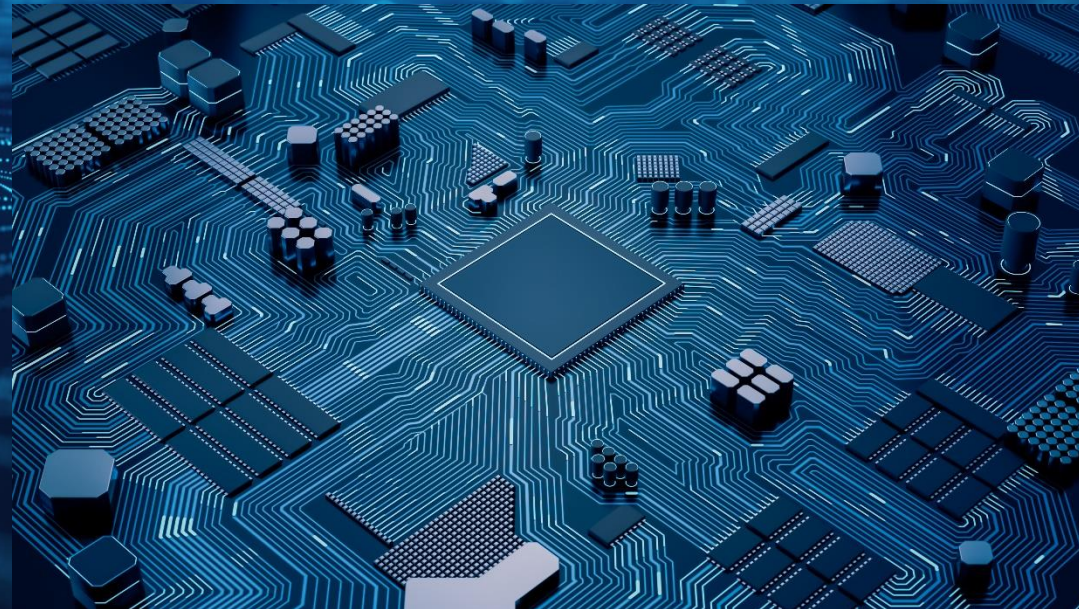


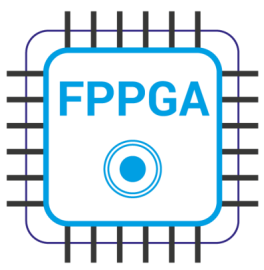
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- [8] D. Pérez , I. Gasulla , J. Capmany J, R.A. Soref. Reconfigurable lattice mesh designs for programmable photonic processors. *Opt Express* 2016, 24, 12093-106.
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- [16] A. Anoni et al. Unscrambling light—automatically undoing strong mixing between modes. *Light Science and Applications* 2017, 6, e17110.
- [17] A. Politi et al. Silica-on-silicon waveguide quantum circuits. *Science* 2008, 320, 646–9.



Programmable Photonics

The Field Programmable Photonics Gate Array

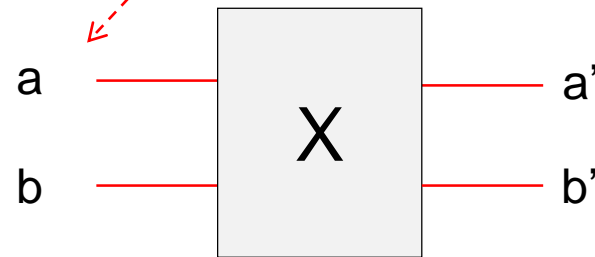
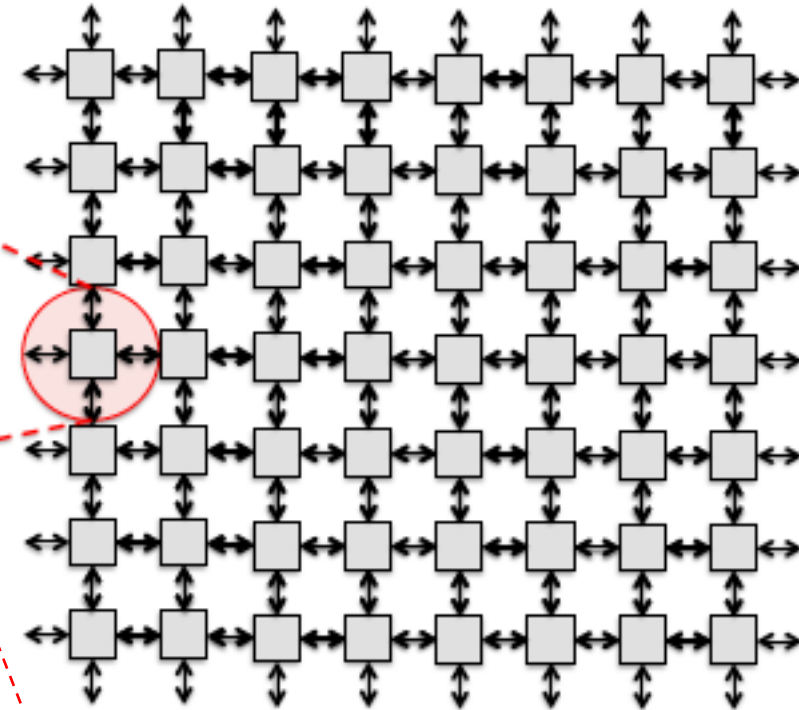
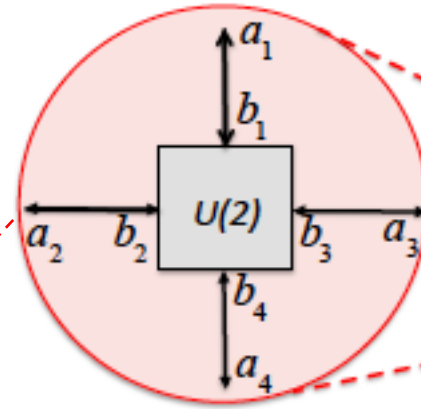




The basics

FPPGAs are built using a 2D mesh of interconnected **reversible 2x2 unitary gates** implementing unitary analog transformations

FPPGAs work with **analog signals** and unitary **2x2 matrix Algebra U(2)**

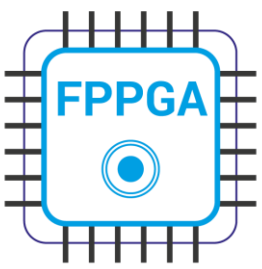


a SWAP b

a	b	a'	b'
0	0	0	0
0	1	1	0
1	0	0	1
1	1	1	1



$$U = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix}$$



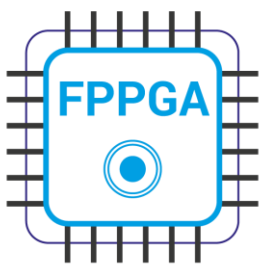
The basics

Reversible gates are built by transforming the **Pauli Matrices**, which are well known in quantum information

$$S_0 = I = \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix}; S_1 = X = \begin{pmatrix} 0 & 1 \\ 1 & 0 \end{pmatrix};$$

$$S_2 = Y = \begin{pmatrix} 0 & -i \\ i & 0 \end{pmatrix}; S_3 = Z = \begin{pmatrix} 1 & 0 \\ 0 & -1 \end{pmatrix}$$

The required transformations are known as **Rotations**



The basics

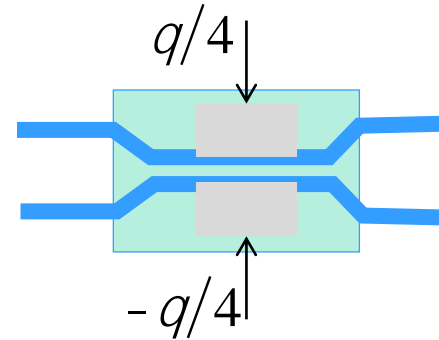
Rotations have simple physical implementations in integrated photonics

$$R_x(q) = e^{-i\frac{q}{2}X} = \begin{pmatrix} \cos(q/2) & i\sin(q/2) \\ i\sin(q/2) & \cos(q/2) \end{pmatrix}$$

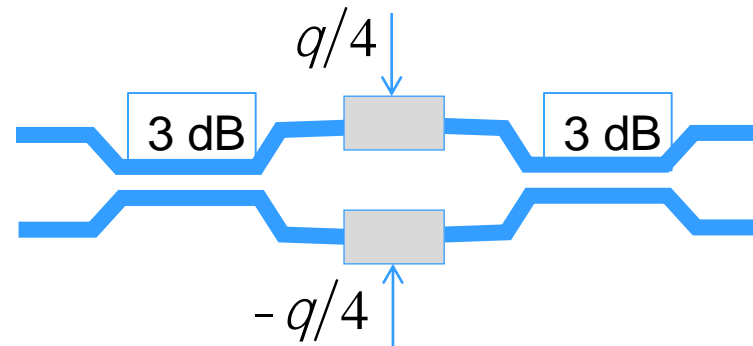
$$R_y(q) = e^{-i\frac{q}{2}Y} = \begin{pmatrix} \cos(q/2) & -\sin(q/2) \\ \sin(q/2) & \cos(q/2) \end{pmatrix}$$

?

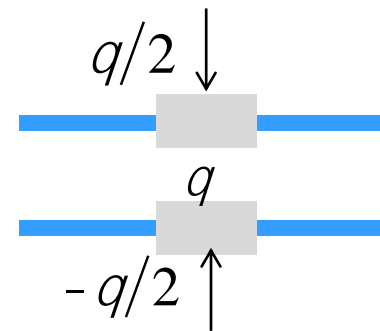
$$R_z(q) = e^{-i\frac{q}{2}Z} = \begin{pmatrix} e^{-i(q/2)} & 0 \\ 0 & e^{i(q/2)} \end{pmatrix}$$



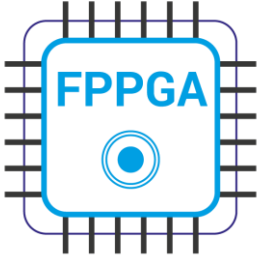
Dual drive directional coupler



Dual drive 3 dB Balanced MZM



Two parallel waveguides with opposite phase shifts



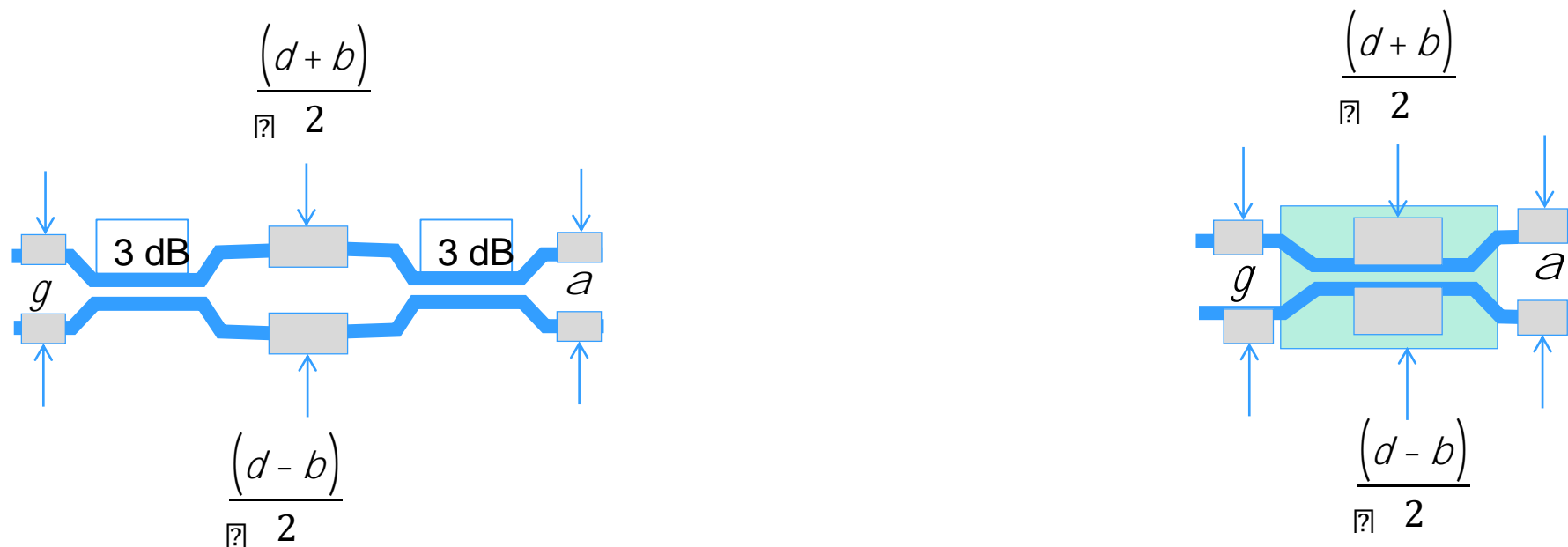
The basics

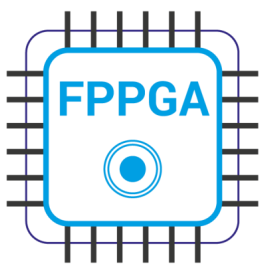
Rotations are key because **any unitary 2x2 matrix transformation** can be obtained using the following cascade of rotation matrices:

$$U = e^{jd} R_z(a) R_y(b) R_z(g)$$

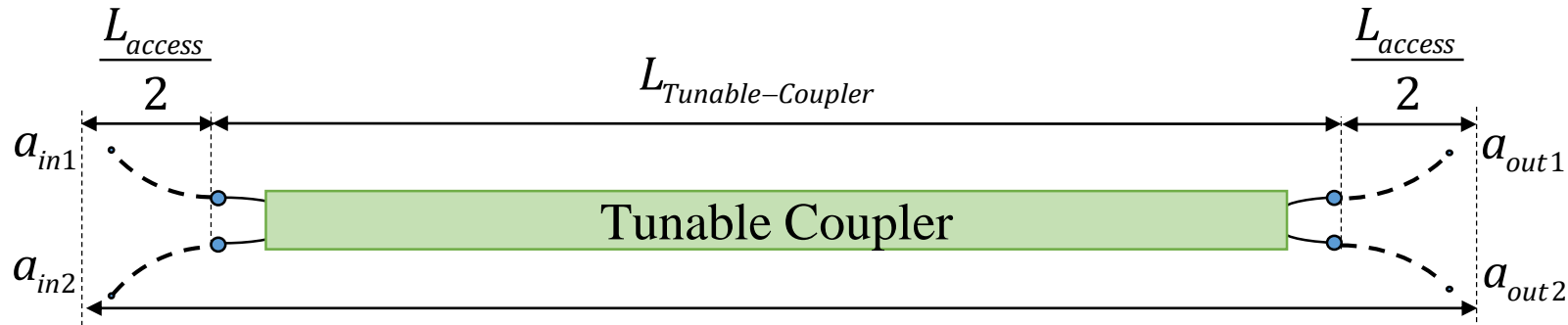
$$U = e^{jd} R_z(a) R_x(b) R_z(g)$$

The former prescriptions (others are possible) allow two options for the compact photonic implementation of any unitary 2x2 matrix



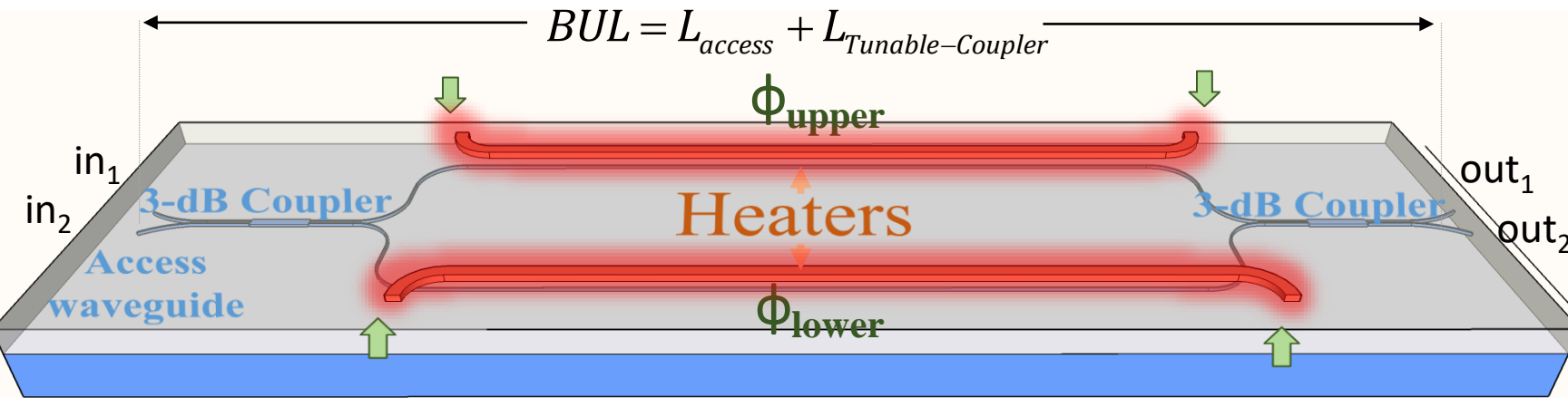


Example: ZYZ implementation

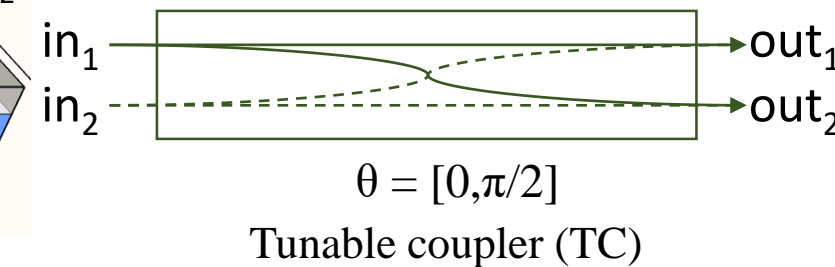
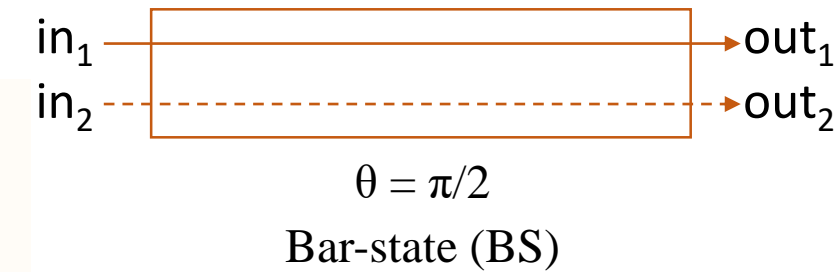
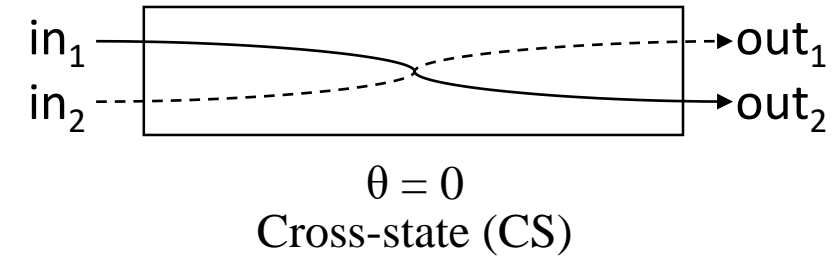


$$BUL = L_{access} + L_{Tunable-Coupler}$$

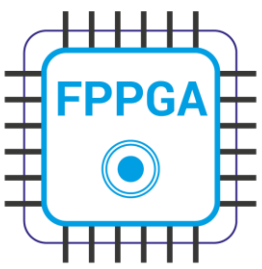
$$BUL = L_{access} + L_{Tunable-Coupler}$$



Control Electronics



TBUs can also be activated by carrier injection modulation



The basics

Feedforward signal processing architectures

Any unitary $n \times n$ transformation can be implemented by means of $n(n-1)/2$ two dimensional unitaries (Hurwitz, 1897).

Ueber die Erzeugung der Invarianten
durch Integration.

Von

A. Hurwitz in Zürich,
correspondirendem Mitgliede der Gesellschaft.

Vorgelegt von dem vorsitzenden Secretär in der Sitzung am 6. März 1897.

- Triangular (Reck et al, 1994)
- Rectangular (Clements et al, 2016)

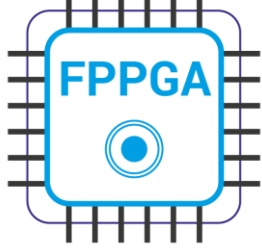
die orthogonale Substitution

$$(15) \quad \begin{cases} x_\alpha &= \cos \varphi \cdot x'_\alpha + \sin \varphi \cdot x'_{\alpha+1}, \\ x_{\alpha+1} &= -\sin \varphi \cdot x'_\alpha + \cos \varphi \cdot x'_{\alpha+1}, \\ x_\beta &= x'_\beta. \end{cases}$$

Nun nehme man $\frac{n(n-1)}{2}$ Winkel

Feedbackward signal Processing architectures

IIR & FIR+IIR structures can be implemented by cascading full 2×2 unitary transformations and partial 1×1 and 1×2 transformations (Pérez et al 2017).

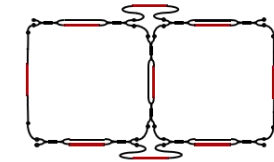
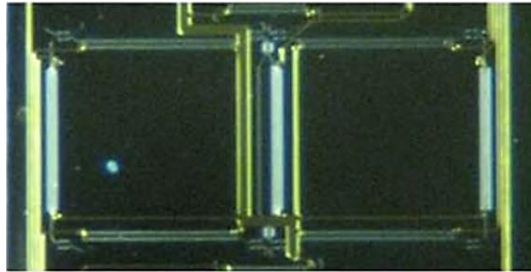


Core Implementations

(a)

2 Square Cells size: 3.5 x 8.5 mm

BUL= 3450 μm $n_g= 1.72$



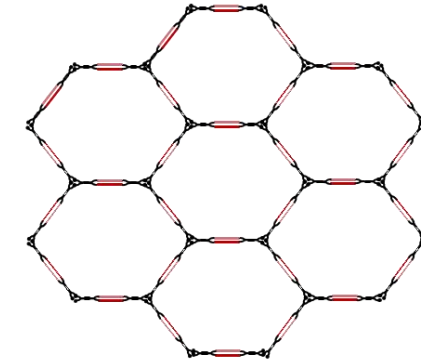
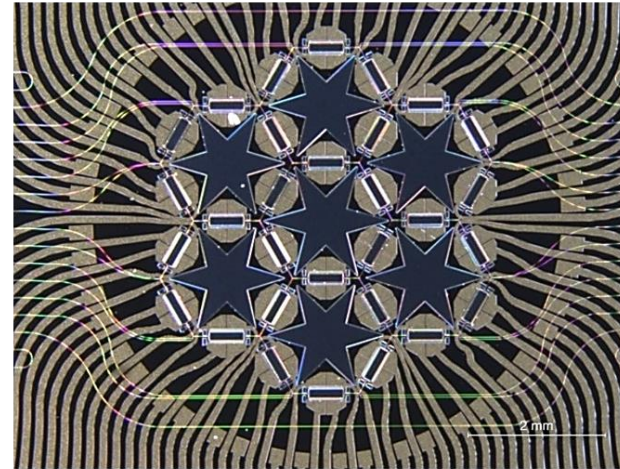
Phase Shifter
Waveguide

Zhuang, et. al.,(2015)

(b)

7 Hexagonal Cells size: 15 x 20 mm

BUL= 975 μm $n_g= 4.18$



Phase Shifter
Waveguide

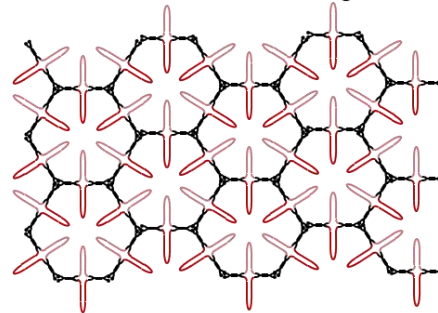
Pérez, et. al.,(2016)

(c)

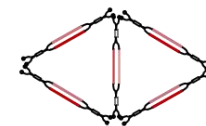
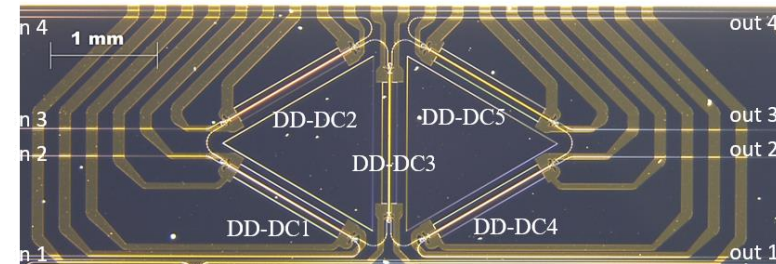
10 Hexagonal Cells size: 5.5 x 11 mm

Pérez, et. al.,(2017)

BUL= 1315 μm $n_g= 1.92$



(d)



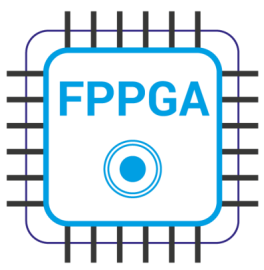
Phase Shifter
Waveguide

Pérez, et. al.,(2019)

Multi-Zennder Interferometer ($\Delta L = 2.00 \mu\text{m}$)

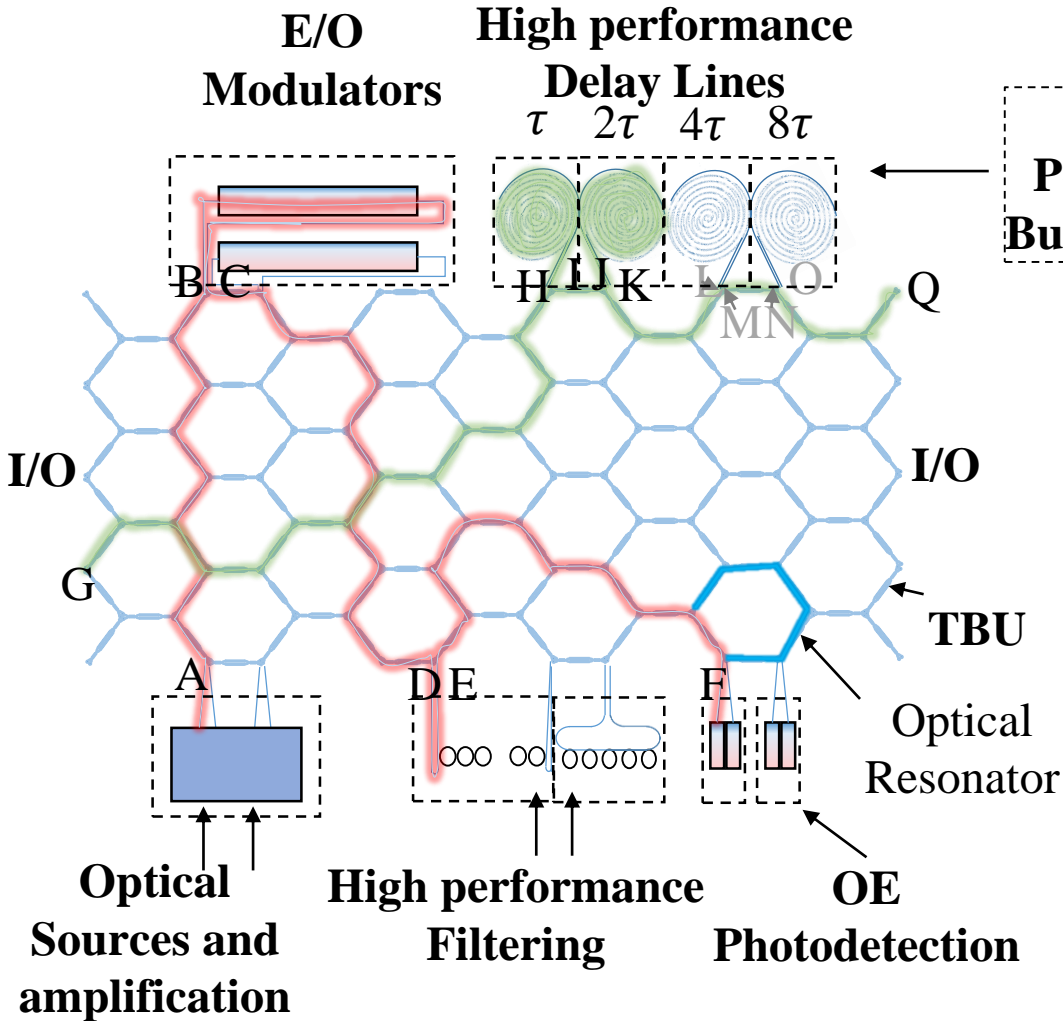
Nature Communications **8**, 636, 2017





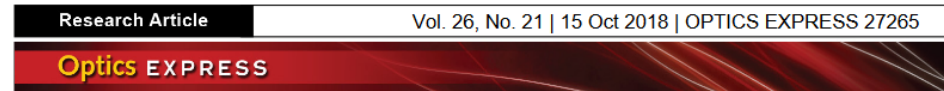
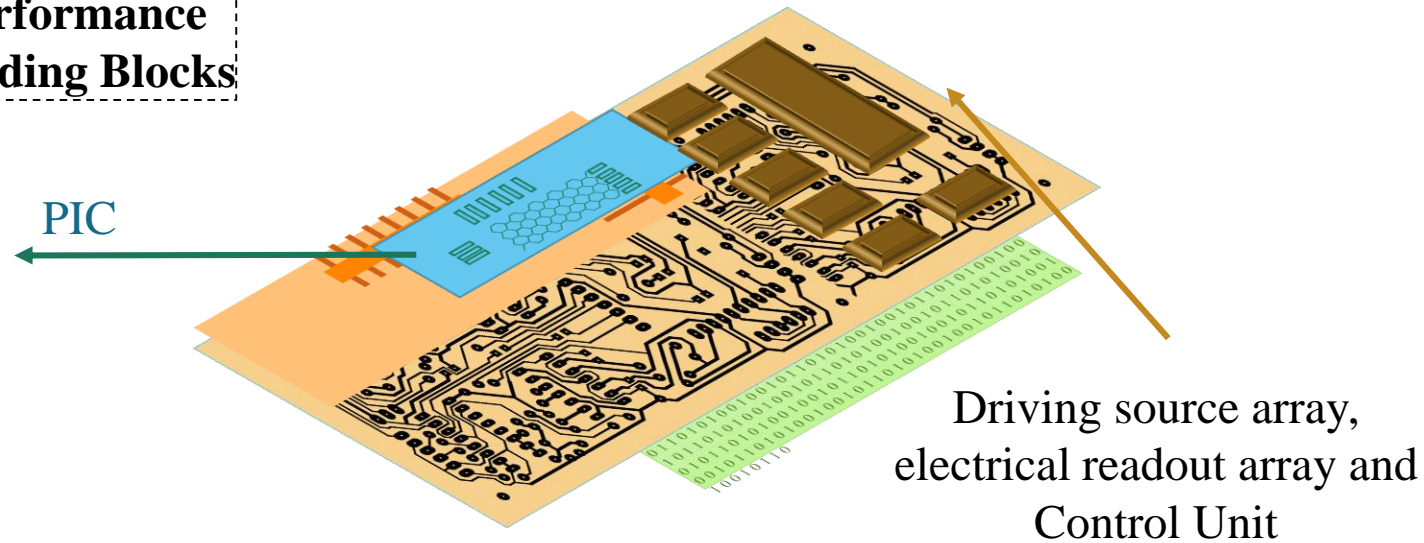
Additional Hardware Elements

- Tier 1: Photonics
- Tier 2: Electronics and RF-mmW
- Tier 3: Software & Control



High-Performance Building Blocks

PIC



Field-programmable photonic arrays

DANIEL PÉREZ, IVANA GASULLA, AND JOSE CAPMANY*

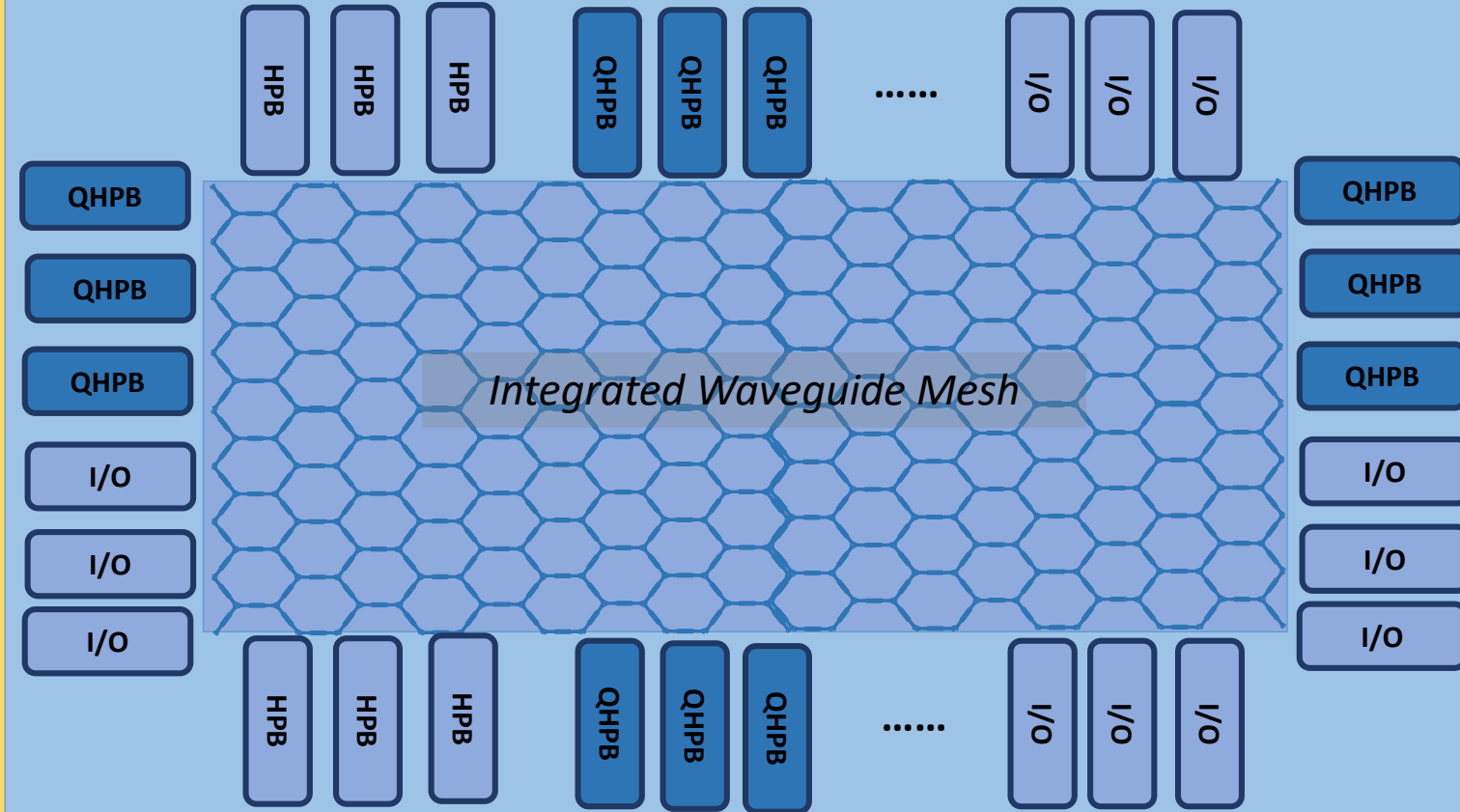
ITEAM Research Institute, Universitat Politècnica de València, Camino de Vera 46022 Valencia, Spain

*jcapmany@iteam.upv.es

Tier #3 Programming/Technology Mapping/Optimization Software

Tier # 2 Control, Monitoring and Driving Electronics

Tier # 1 Integrated Photonics



Tier 3
(Software)

Programming

Technology
Mapping

Optimization

Tier 2
(Electronics)

Driving

Control &
monitorng

Tier 1
Photonics

Quantum
devices

Classical
devices

**Waveguide
Mesh**

HPBs

I/O

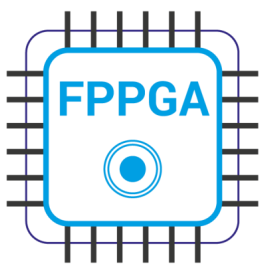
QHPBs

Quantum devices

- Spiralled nanowire SFWM single Photon sources
- CROW single photon SFWM sources
- Integrated Bragg+ Ring cavity SFWM single Photon sources
- Integrated Single photon detectors
- Ancilla qbit readers

Classical devices

- NxN programmable Linear mode transformers
- Tunable filters
- Switches
- Delay lines
- Photodetectors
- Optical sources
- Tunable filters
- Switches
- Modulators
- Delay lines
- Chip-chip couplers
- Chip-fiber couplers



Hardware Scalability challenges



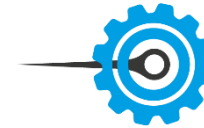
Power consumption
Accumulated optical loss



Electrical Interfacing
System integration

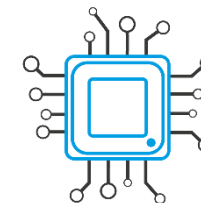


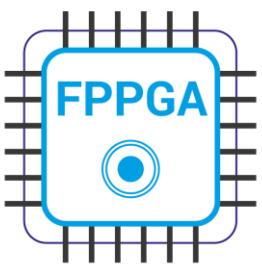
Optical monitoring points.



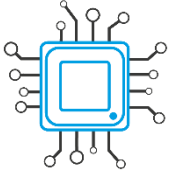
Optical crosstalk
Tuning crosstalk

Some of them can be mitigated by a smart software layer and thanks to the massively interconnected nature of the FPPGA core.





Software Challenges



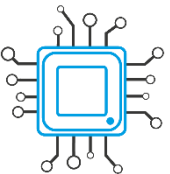
Control and operation based on **global algorithms and presets**

- Requires the pre-characterization of the FPPGA core.
- Includes preset configurations, auto-routing algorithms, user-defined configurations.



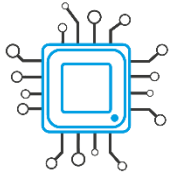
Control and operation based on **computational optimization algorithms**

- Enables *self-configuring, self-healing, black-box optimizations* and *mitigates non-ideal operation* of photonic components.



High Level Description and specification language

- To enable the high-level programming of the FPPGA resources.



Control and operation based on global algorithms and presets

Develop / compute control vectors for each configuration:

$$C_1 = [H01_U, H01_D, H02_U, H02_D, \dots, H30_D]$$

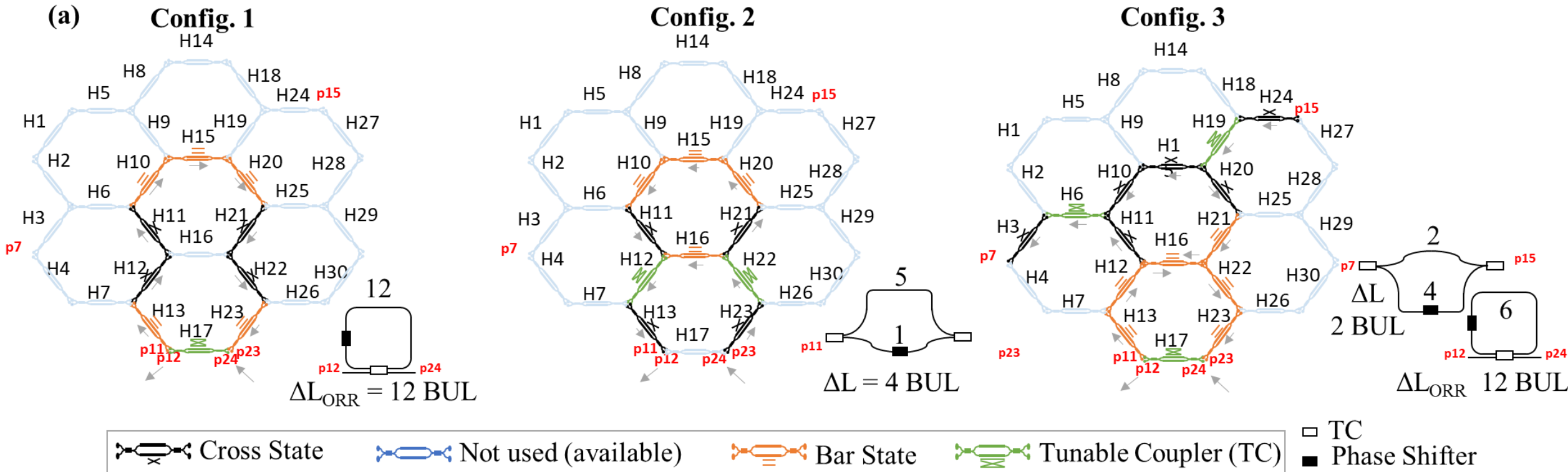
$$C_2 = [H01_U, H01_D, H02_U, H02_D, \dots, H30_D]$$

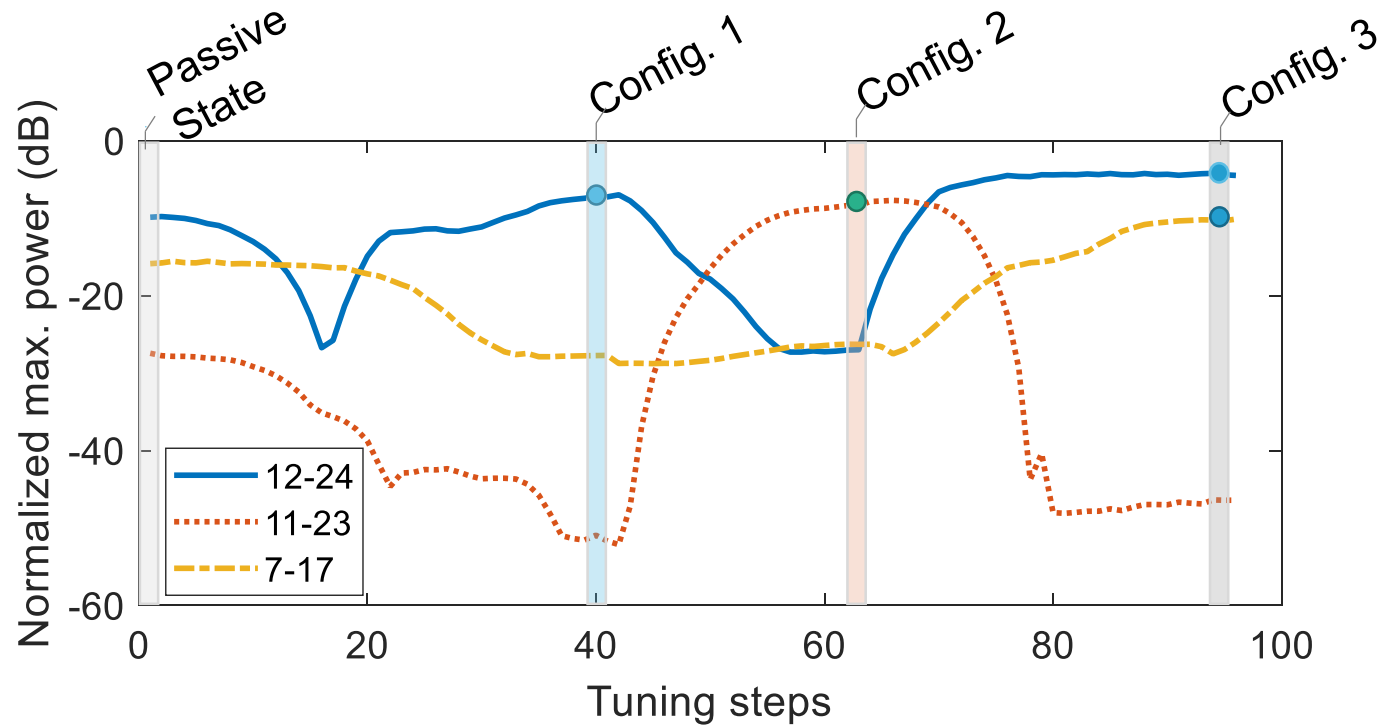
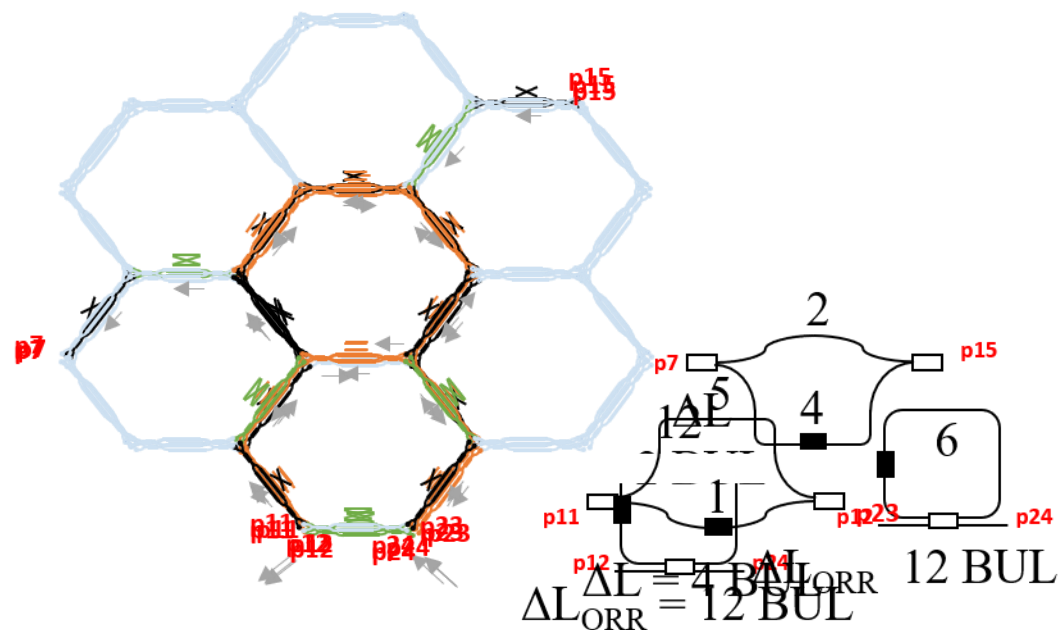
$$C_3 = [H01_U, H01_D, H02_U, H02_D, \dots, H30_D]$$

Predefined pre-sets.

A. López et al., presented at ECOC 2019.

J. Capmany, D. Pérez, "Programmable Integrated Photonics", in press Oxford University Press (2019)



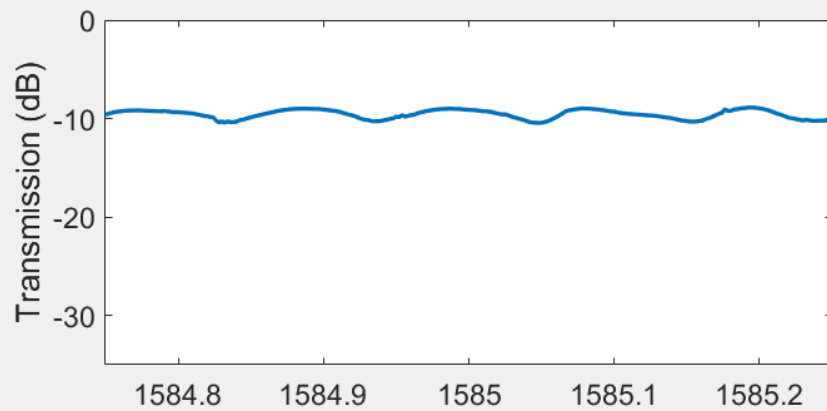
Config. 1

Cross State

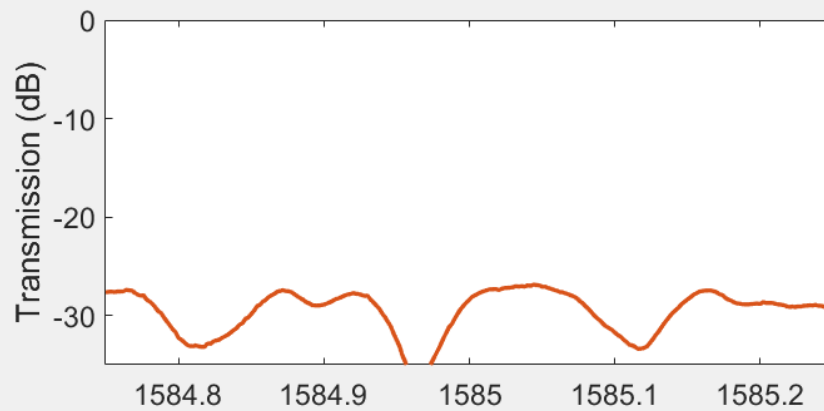
Not used (available)

Bar State

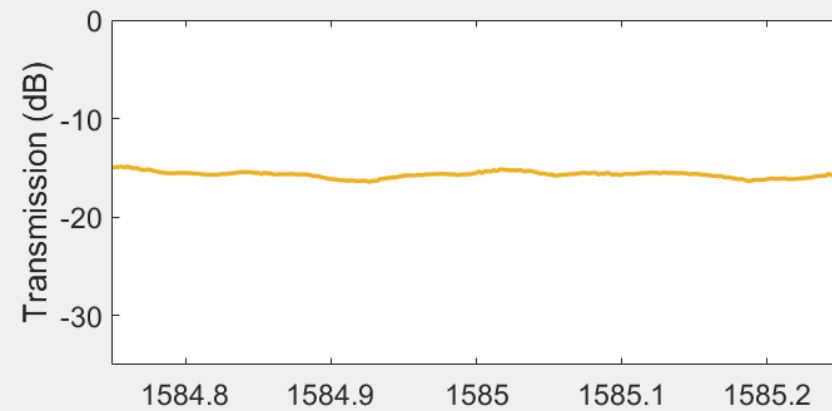
Tunable Coupler (TC)

 TC
 Phase Shifter


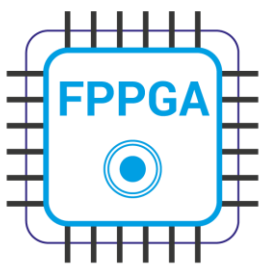
1p.12-p.24



1p.11-p.23



1p.7-p.15



Applications



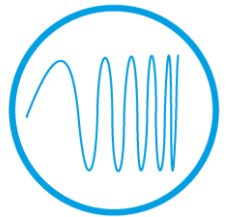
5G and Beyond



Bio instruments



Internet of Things



HW acceleration



Transport



Sensors

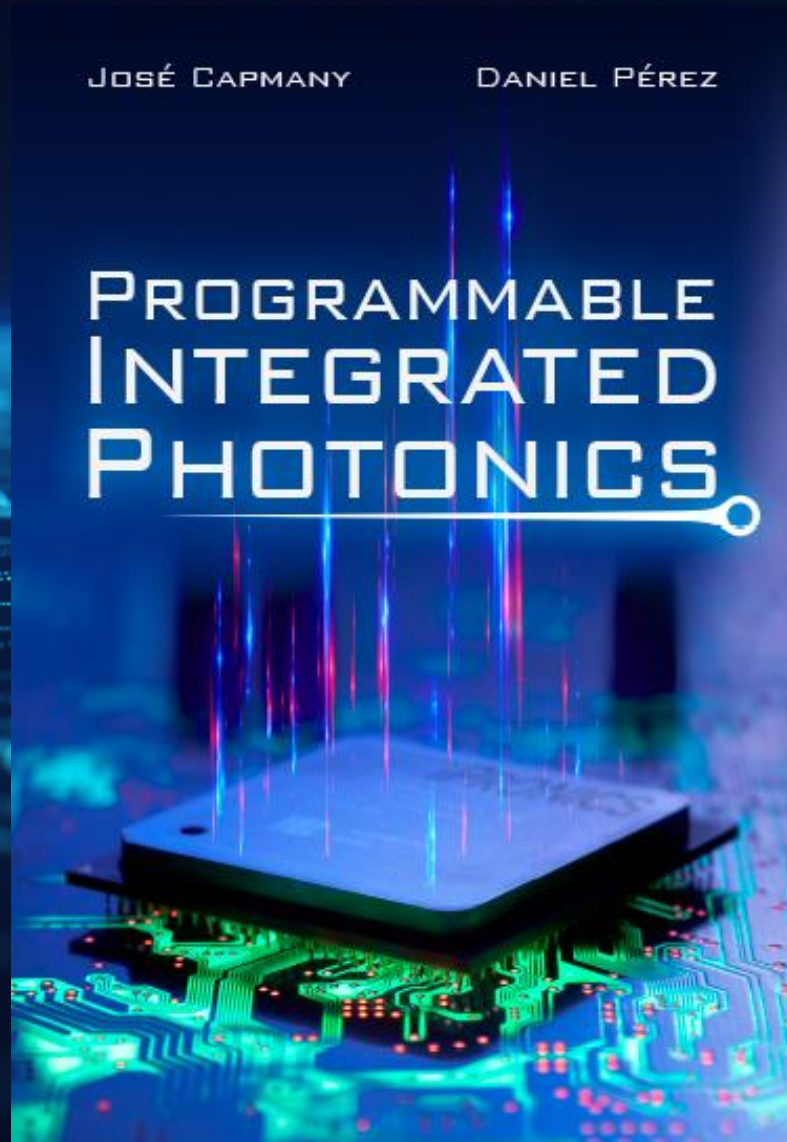


Neurocomputing
and AI



Quantum
Information

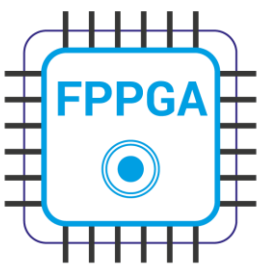
More Information?, stay tuned



Jan-Feb 2020

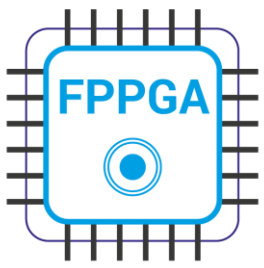
Summary, Conclusions & Take Away Messages





Summary and Conclusions

- MWP is becoming a key enabling technology in a variety of application scenarios
- For efficient penetration into these photonic **integration is key**
- A considerable number of Application Specific Photonic Integrated Circuits (**ASPICs**) **have** been reported with **a limited degree of functionality**
- Functionality and cost efficiency can be improved **by** means of **reconfigurability**. A general purpose programmable chip for MWP applications is under current R&D
- **Programmable chips with** the incorporation of **extra elements** (IP blocks, control electronics and specialized software) **enable the equivalent of the electronic FPGA**
- The FPPGA relies on different basic operations (analog vs digital) compared to electronics, but these are required to handle lightwave signals
- FPPGA applications span a myriad of fields other than MWP



Take Away Messages



Programmable Photonics is going to happen, YES or YES.

It shares commonalities with integrated Electronics

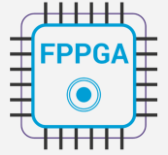
Yet it is completely different



INVENT THE FUTURE OF PHOTONIC INTEGRATION

www.ipronics.com

Programmable
Photonic Protocols



AI-Machine
Learning- algorithms



Advanced
Optimization Routines



UNIVERSITAT
POLITÈCNICA
DE VALÈNCIA

Oct 2019

Support \mathcal{W} iegraphs

Examples & extra technical material





Landmarks in programmable electronics

1948

Transistor

Shockley Brattain,
Bardeen

1957

Fairchild

Fairchild, Noyce, Moore. *Integrated circuit, Moore's Law*

1972

INTEL

Hoff, Faggin, Shima, Mazor,
8080 microprocessor

1984

XilinX

Freeman &
Vonderschmitt, *FPGA*

1956

Shockley Semiconductors

Shockley, Bob
Noyce and
Gordon Moore

1968

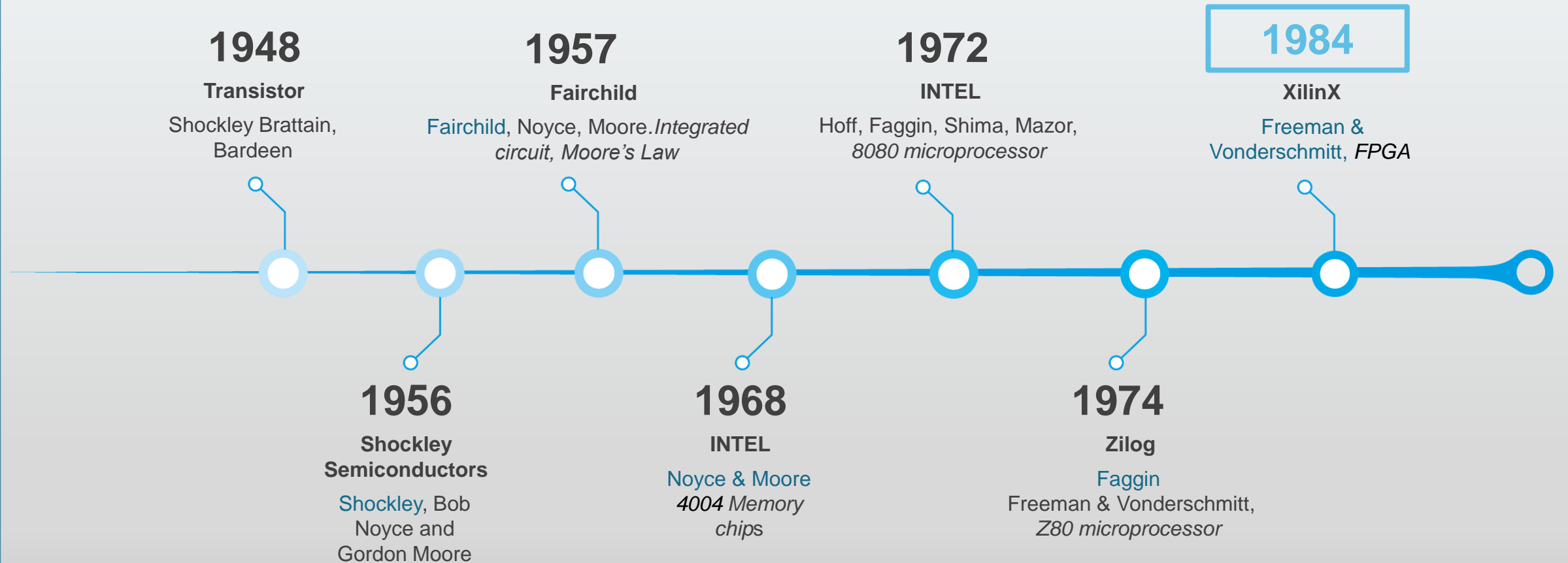
INTEL

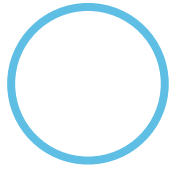
Noyce & Moore
4004 Memory chips

1974

Zilog

Faggin
Freeman & Vonderschmitt,
Z80 microprocessor





Is the right time for FPPAS?

Electronics

Age of Invention

- Cost containment
- Maximize efficiency in cost & functionality
- Eliminate waste in logic blocks
- Design efficient 2D interconnection
- Manual design, placement & routing
- Multi-Chip partitioning

(1984-1991)

Age of Expansion

- Moore law enabled doubling the size of largest FPGAs and halving cost per function (area less precious)
- Smaller & simpler logic units/more complex logic blocks
- Longer connections not only nearest neighbors
- Design automation (placing, routing synthesis) essential
- Increase in addressable ASIC market

(1992-1999)

Age of Accumulation

- Larger size FPGAs are no longer essential
- FPGAs include logic function + High performance predefined building dedicated blocks interconnected
- Customized products for communications

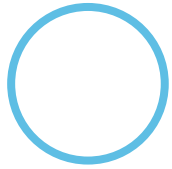
(2000-2007)

Photonics

Age of Invention

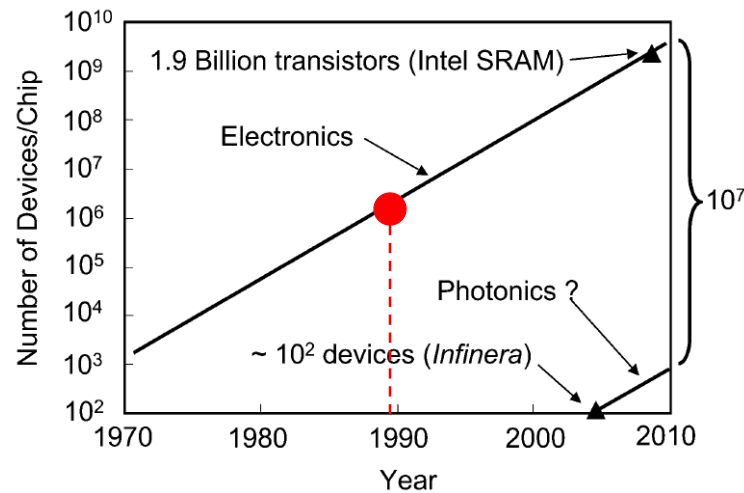
- Material technology platform
- Maximize efficiency in cost & functionality
- Define photonic analog gates/locks
- Design efficient 2D interconnection meshes
- Manual design, placement & routing
- Automatic control, bias, monitoring
- Interfacing with RF and electronic bias

(2015-2022)

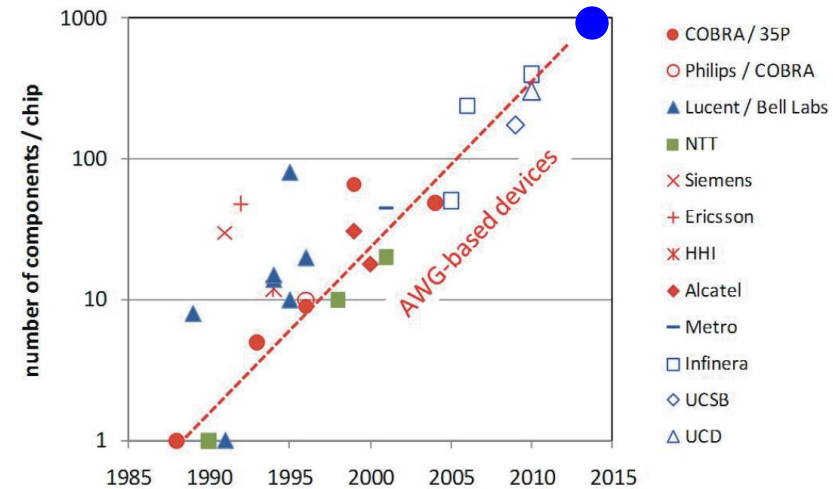


Is the right time for FPPAS?

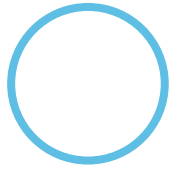
$$\frac{\text{Photon Wavelength}}{\text{Electron Wavelength}} \gg 10^3 \Rightarrow \frac{\text{Photonic Integration density/surface unit}}{\text{Electronic Integration density/surface unit}} \gg 10^{-3}$$



Integration density when
FPGA was proposed 10^6

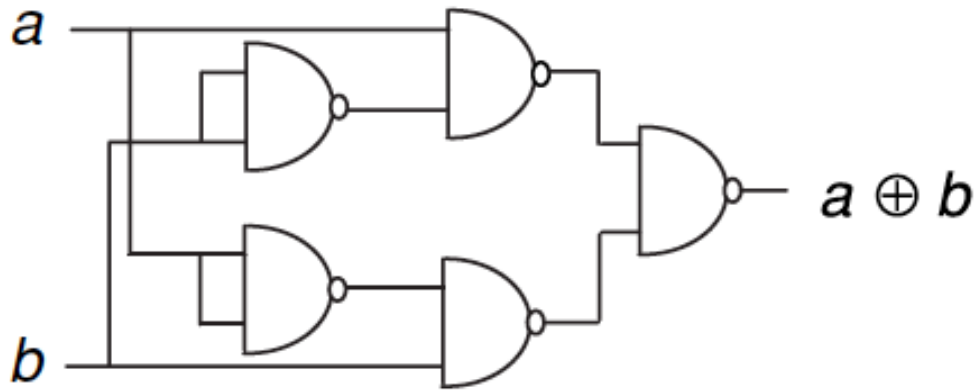


Equivalent Integration density when
FPPGA have been proposed $10^6 \times 10^{-3} = 10^3$



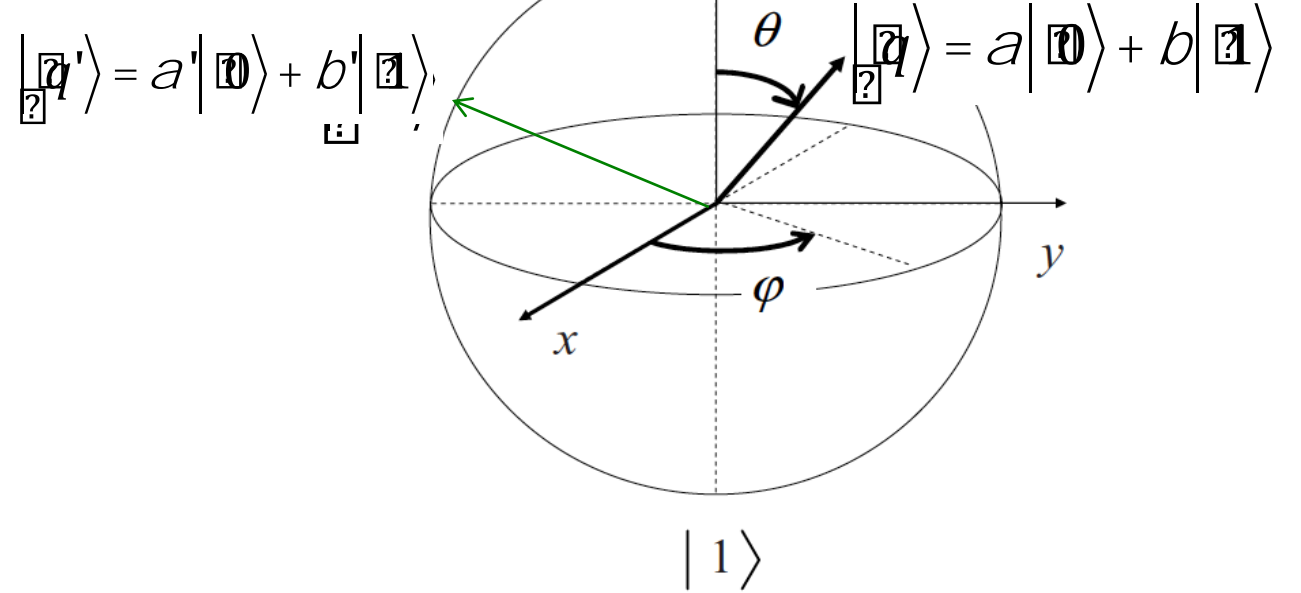
Analog vs Digital Bit Processing

Digital Electronics



XOR

Quantum Optics



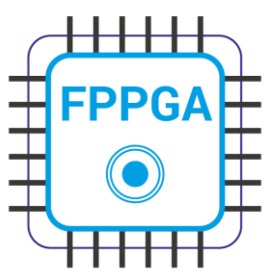
Qubits are **analog** processed (amplitudes), using the rules of 2x2 unitary Matrix Algebra

In digital electronics, bits 0 and 1 are **digitally** processed using the rules of **Boolean Algebra**

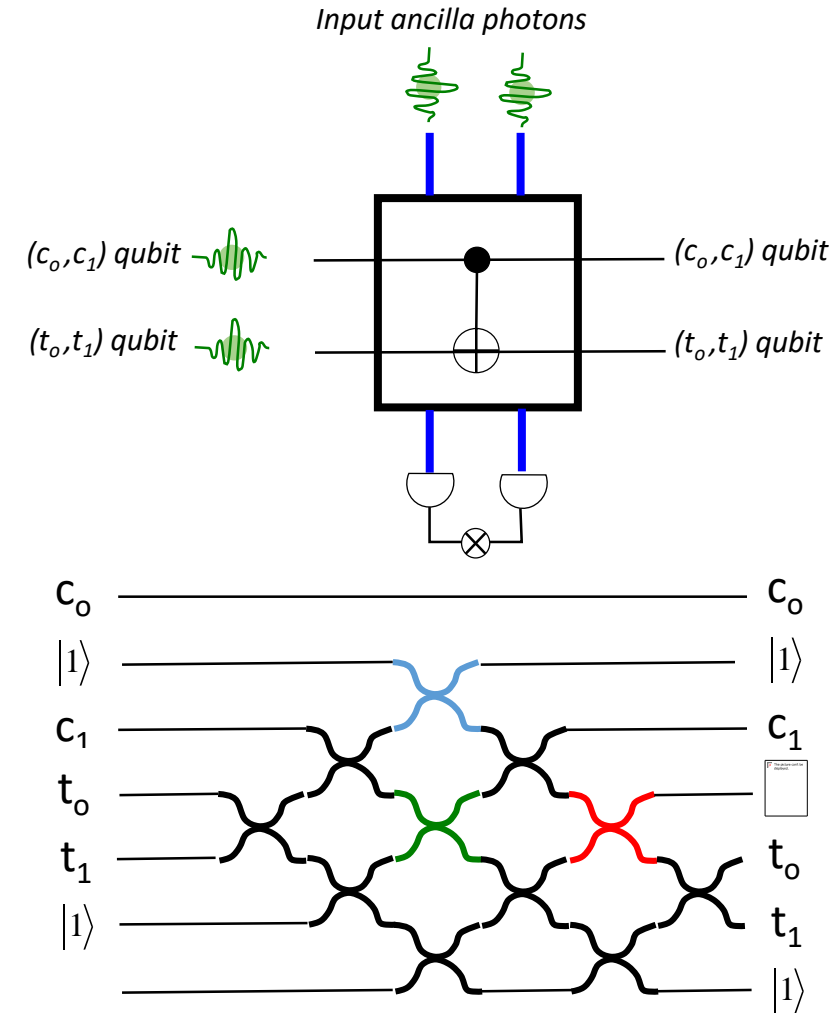
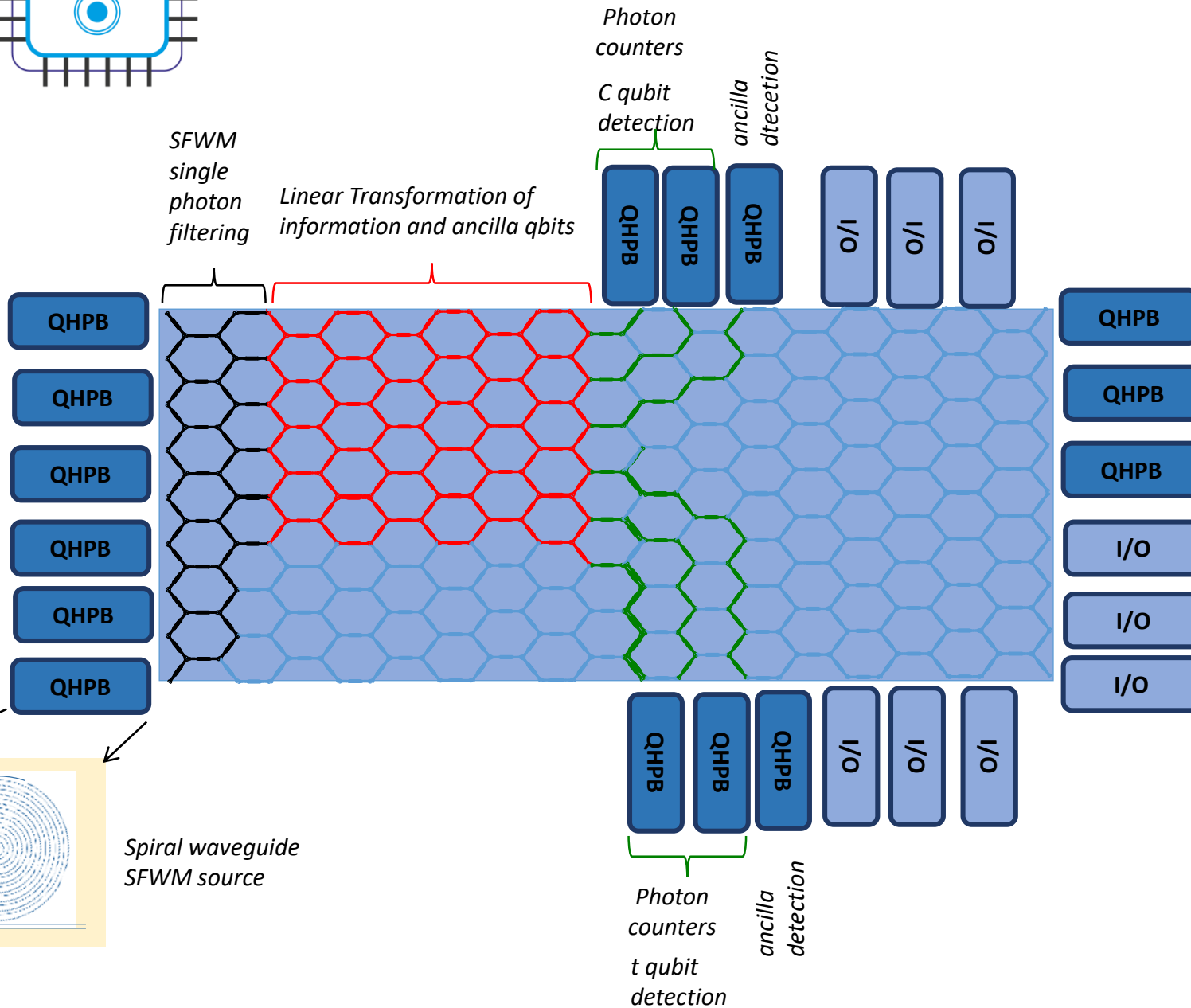
$$y = f(a,b)$$

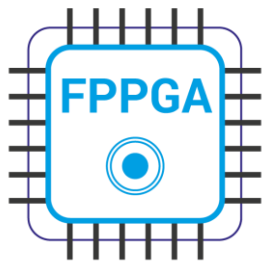
$$a,b = \{0,1\}$$

$$\begin{pmatrix} a' \\ b' \end{pmatrix} = \begin{pmatrix} u_{11} & u_{12} \\ u_{21} & u_{22} \end{pmatrix} \begin{pmatrix} a \\ b \end{pmatrix}$$

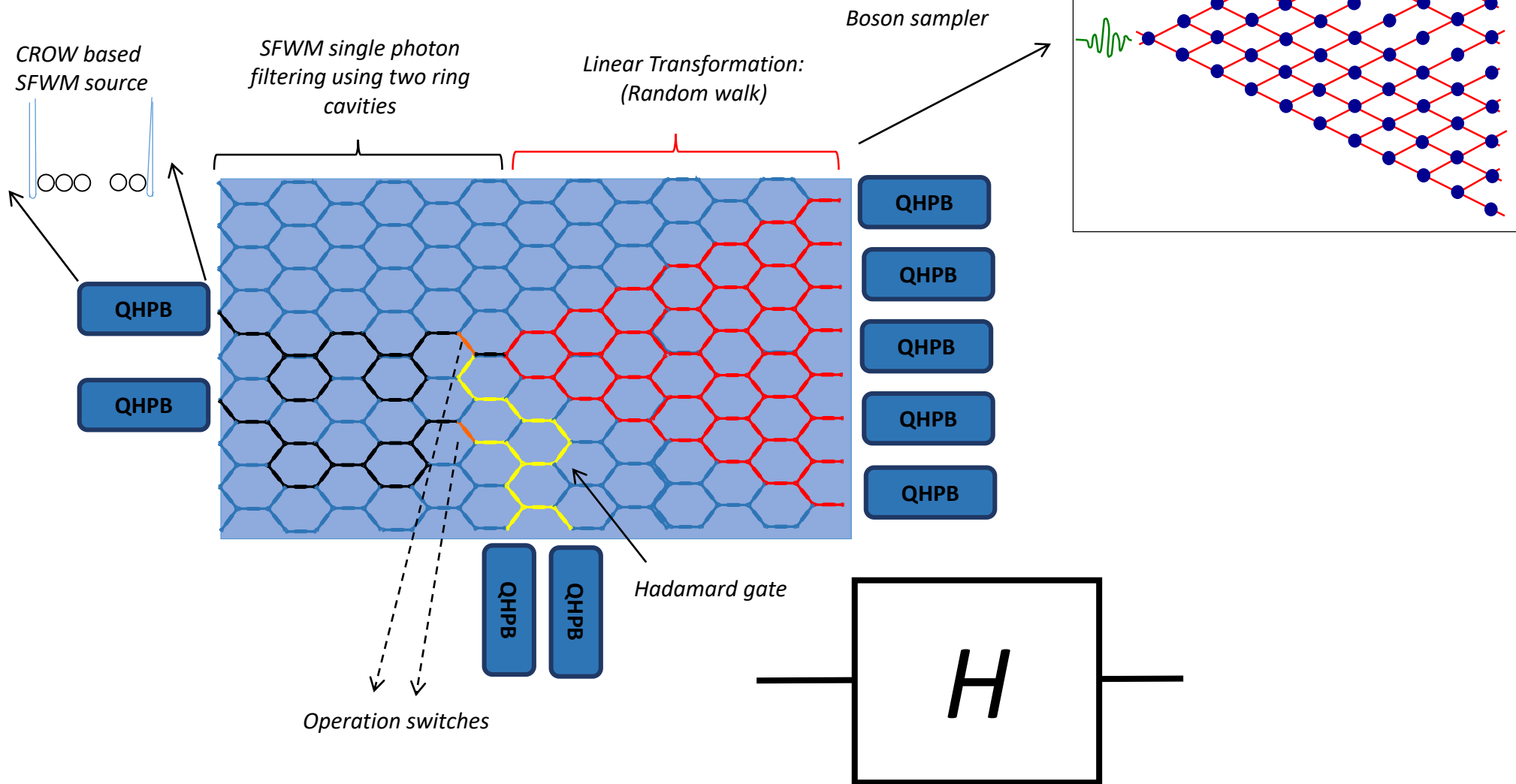


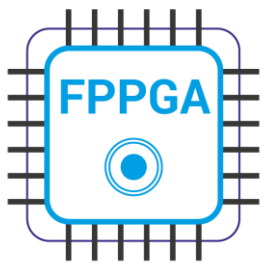
Example 1: Heralded CNOT Quantum Gate implementation



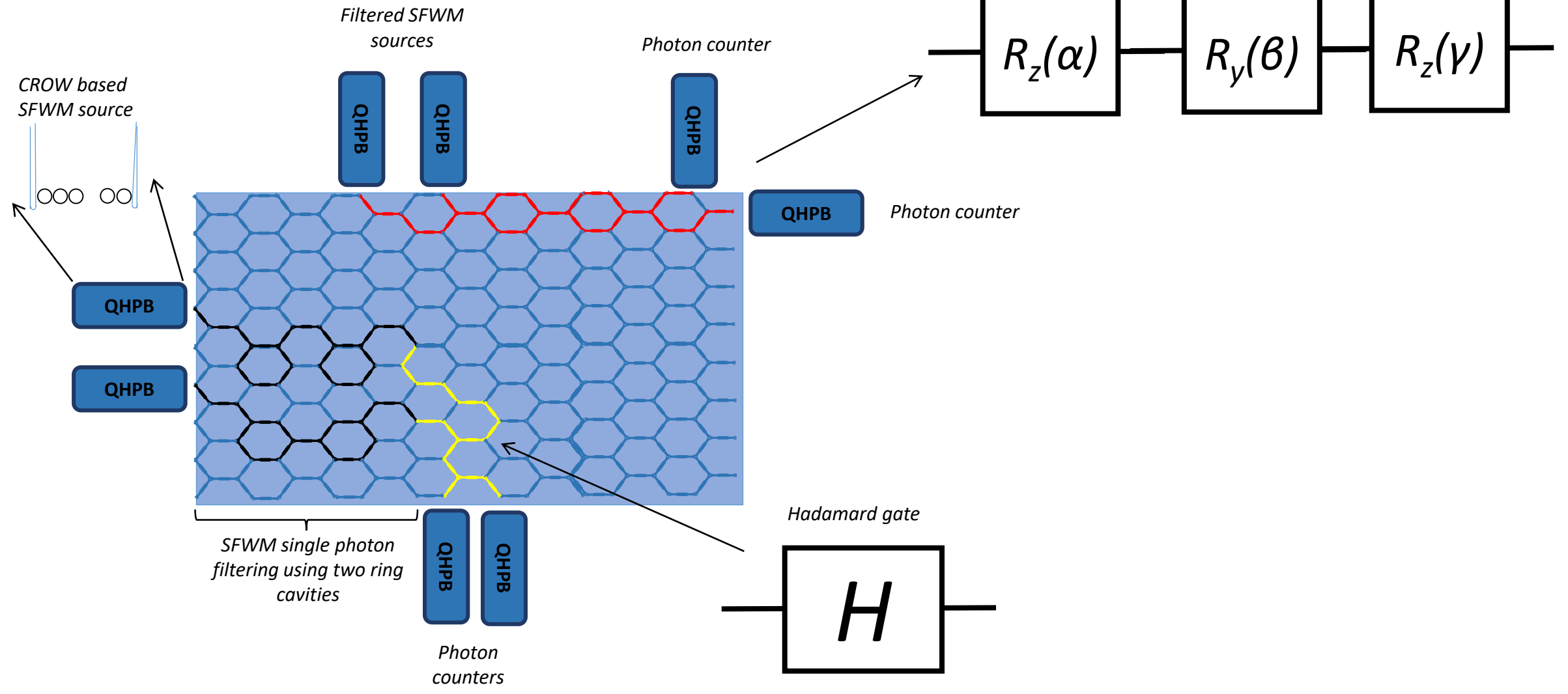


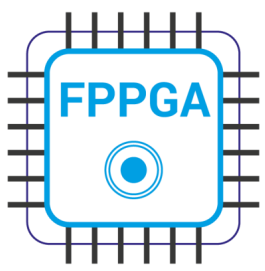
Example 2: Switched quantum circuits (Boson Sampler & Hadamard gate)





Example 3: Simultaneous quantum circuits (Rotation cascade and Hadamard Gate)



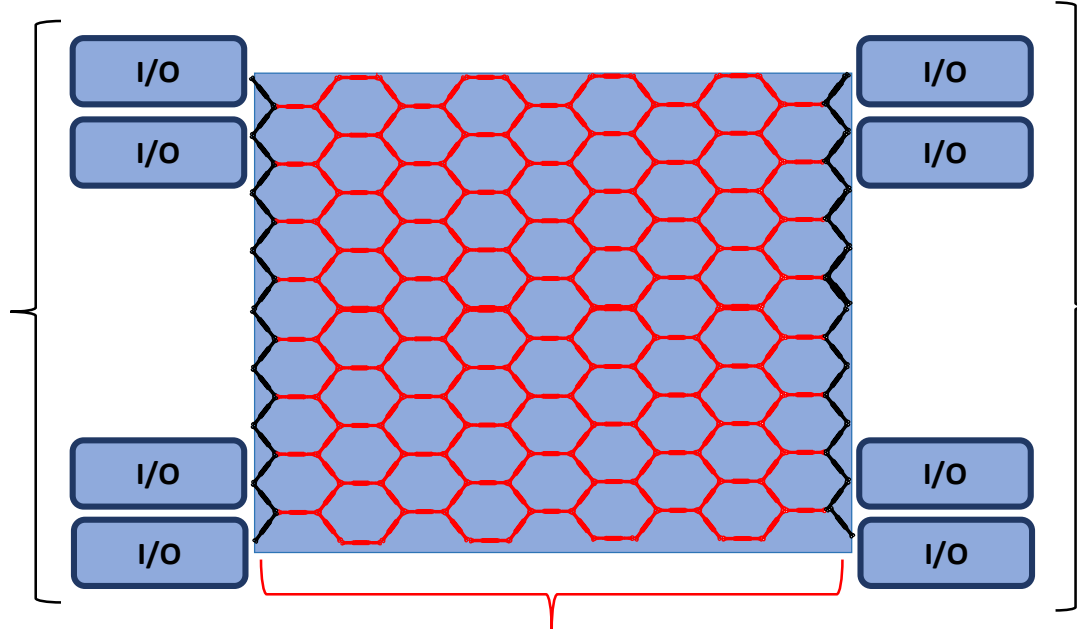


Example 4: Quantum Fourier Transformer

Input state

$$|\psi\rangle = \sum_{k=0}^{N-1} x_k |k\rangle$$

$$|k\rangle = \begin{pmatrix} 0 \\ \vdots \\ 1 \\ \vdots \\ 0 \end{pmatrix} \quad \downarrow \text{K+1 row}$$

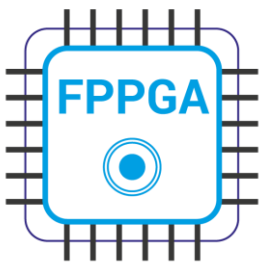


Unitary matrix for QFT

$$M = \frac{1}{\sqrt{N}} \begin{pmatrix} 1 & 1 & 1 & 1 & 1 \\ 1 & \omega & \omega^2 & \dots & \omega^{N-1} \\ 1 & \omega^2 & \omega^4 & \dots & \omega^{2(N-1)} \\ 1 & \vdots & \vdots & \ddots & \vdots \\ 1 & \omega^{N-1} & \omega^{2(N-1)} & \dots & \omega^{(N-1)(N-1)} \end{pmatrix}; \quad \omega = e^{i\frac{2\pi}{N}}$$

Output state

$$|\tilde{\psi}\rangle = \text{QFT}|\psi\rangle = \sum_{k=0}^{N-1} \sum_{n=0}^{N-1} M_{nk} x_k |k\rangle$$



Example 5: Simultaneous quantum & classical circuits (Rotation cascade and SCISSOR)

